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DisplayPort Compliance Test Update

Granite River Labs
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Agenda

- DP/DPC 1.4 Compliance Test
- DP 1.4 up-to-date requirements
- DP/DPC 1.4 Electrical Test Method

DP/DPC 1.4 Compliance Test

- Test plan depends on device type and supported features.
- Requirements change. Your ATC can keep you up to date.

DPC 1.4	**Power Delivery Electrical Tests**	
	Power Delivery Protocol Tests (including Device Pin Assignments Verification)	
	VBUS and VCONN Verification	
	PHY Crosstalk Test 2+2 (DP & USB)	
	Billboard Test	
	DP 1.4 (Std, Mini)	**DisplayPort Main link Electrical Tests**
		DisplayPort Aux channel PHY
		Link Layer Test
		EDID
		Interoperability
		Multi-Stream Transport (MST)

Notes :

1. DP 1.4 silicon must support **Swing level 3**.
2. Rx DPCD Error checking available and functioning via AUX channel.

DP/DPC 1.4 Compliance Test

- Source –
  - All DP 1.2 CTS for HBR2 and lower line rates – follow current program
  - **HBR3 main link PHY compliance – factoring latest PHY subgroup proposal**
  - **Prove link training and functional verification at HBR3**
    - Reference Sinks: RealTek, Mstar
- Sink -
  - All DP 1.2 CTS for HBR2 and lower line rates – follow current program
  - **HBR3 sink jitter tolerance**
  - **Prove link training and functional verification at HBR3**
    - Reference Source: AMD RX480
  - **Symbol error count registers available and functioning via AUX channel (no special programs to access error count)**

DPC requirements information

- DPC certification required USB PD controller TID and related chipset information.

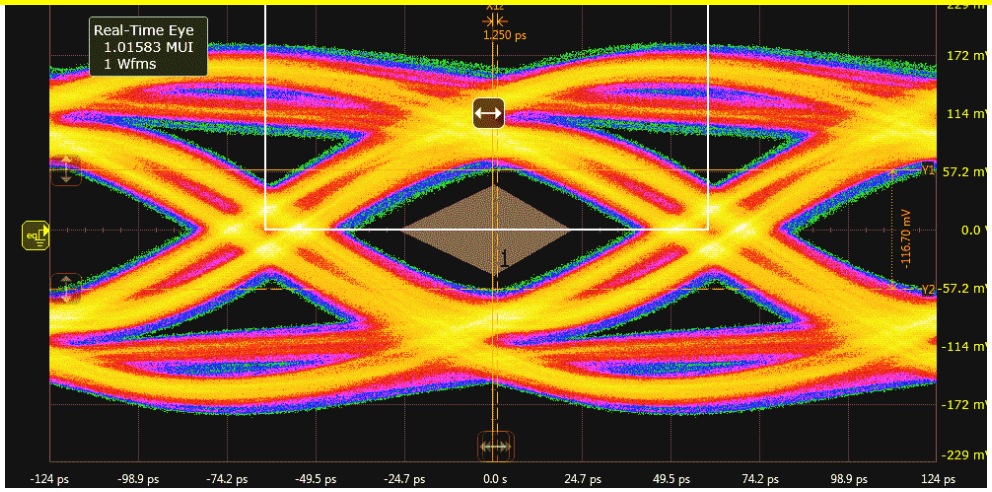
Product name	Silicon Vendor	Model	TID
USB PD Controller	Cypress	CYPD4125	1098024
DP Silicon	Intel	Gemini Lake	N/A
MUX used	Parade	PS8743B-B1	N/A
USB Silicon	Intel	Gemini Lake	N/A

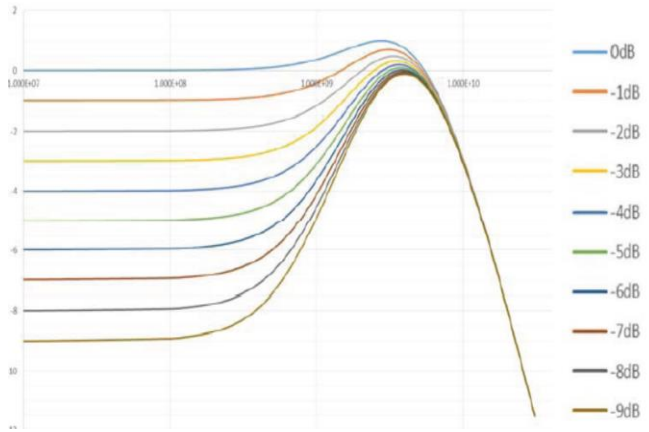
- Pin assignment E must be supports both on Source and Sink.

DP 1.4 up-to-date requirements

- **Requirement of Electrical test**
  - Tx HBR3 Discovery of the optimized CTLE setting and meeting new eye height and Jitter requirements.

HBR3 TP3_CTLE Waveform EYE Height (EH): **≥65mV_diff_pp**

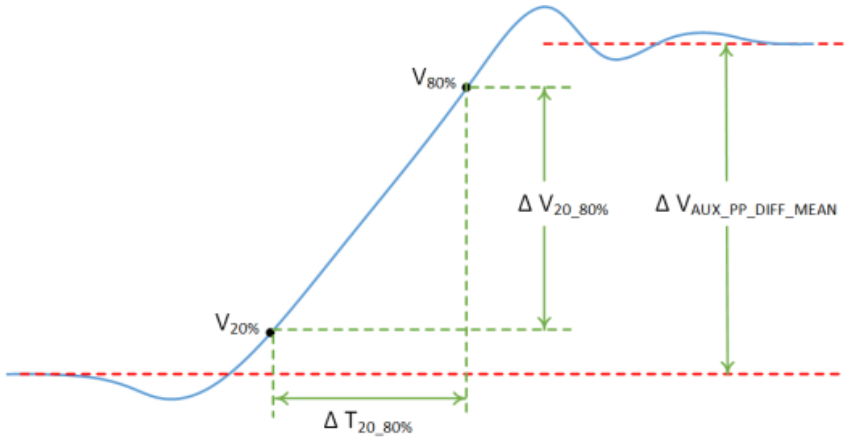




  - Tx HBR2/HBR3 Level and Equalization is going to be tested with Scope using **spectral method.**

DP 1.4 up-to-date requirements

- **Requirement of Aux channel Electrical test**
  - Additional Aux channel Slew rate test.



AUX Slew Rate (20-80%) ≤ 375mV/ns

DP 1.4 up-to-date requirements

- **Requirement of Link Layer**
  - LT fallback and reduce lane count test will be required test items.

(Reduced Lane Count, Test 1) CR failure on Lane2/3
(Reduced Lane Count, Test 2) CR failure on Lane1/2/3
(Reduced Lane Count, Test 3) Symbol Lock failure on Lane2/3
(Reduced Lane Count, Test 4) Symbol Lock failure on Lane1/2/3
400.1.1 HPD Event Pulse Length Test
400.1.2 IRQ_HPD Pulse Length Test
400.1.3 Inactive HPD / Inactive AUX Test
400.2.1 Link Training CR Fallback Test
400.2.2 Link Training EQ Fallback Test

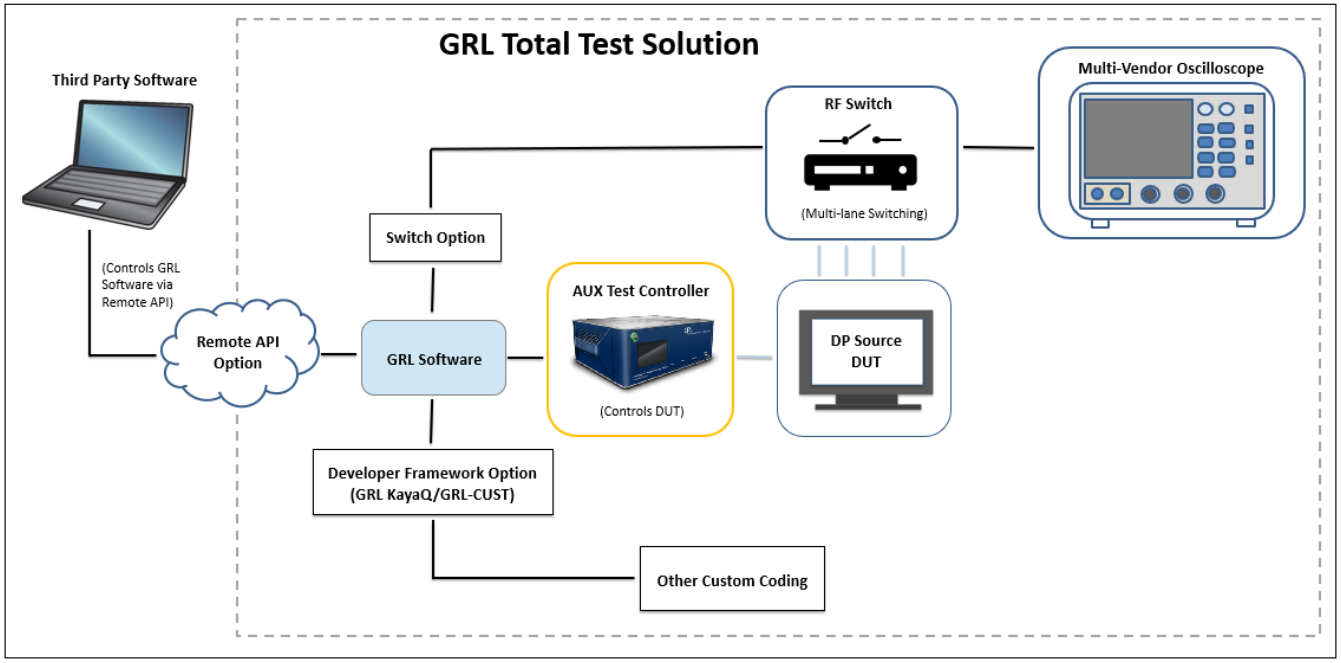
  - Chapter 7 of Sink Link Layer Test becomes required test items

7.2.1.1 Sink Organizationally Unique Identifier (OUI)
7.2.1.2 Sink count
7.2.1.3 Sink Status
7.2.1.4 Symbol Error Count
7.2.1.5 Device Identifications
7.2.1.6 Number of Receiver Ports
7.2.1.7 Main Link Channel Coding

- HDCP 2.2 is required to be tested if implemented.
- (upcoming) DP 1.4 LL test will be performed with QD980 or UCD-400.

DP 1.4 HBR3 Source Spectral Test

1. Acquire Waveform
2. Analyze Waveform
3. Support Multi-vendor Oscilloscope.
4. Advantage of the S/W: Run both GRL and test app of scope simultaneously.



'Source Spectral Test' is a New Source (Chap 3) Requirement
GRL has an Approved VESA MOI we use in the Lab prior to TE Vendors

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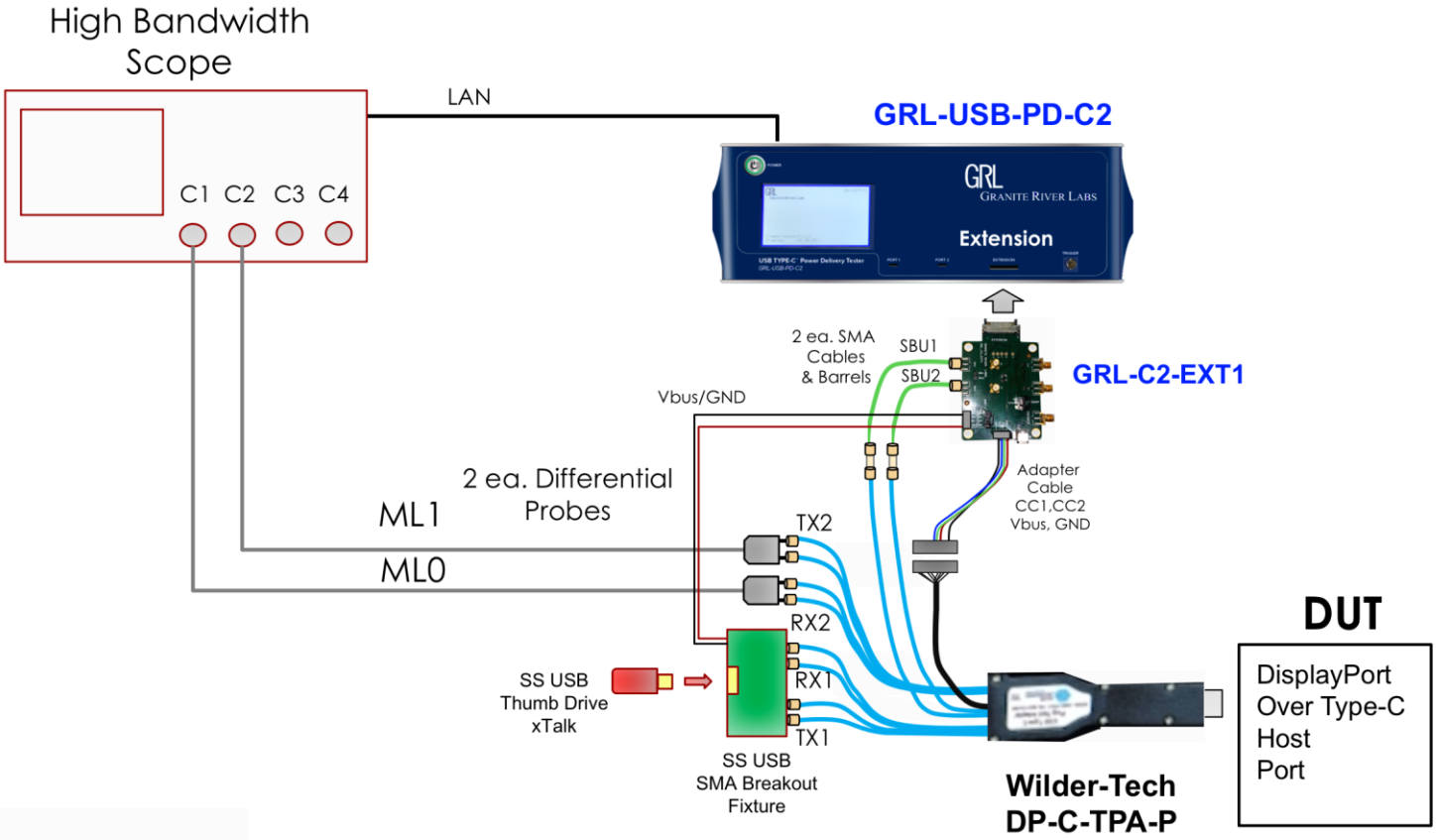
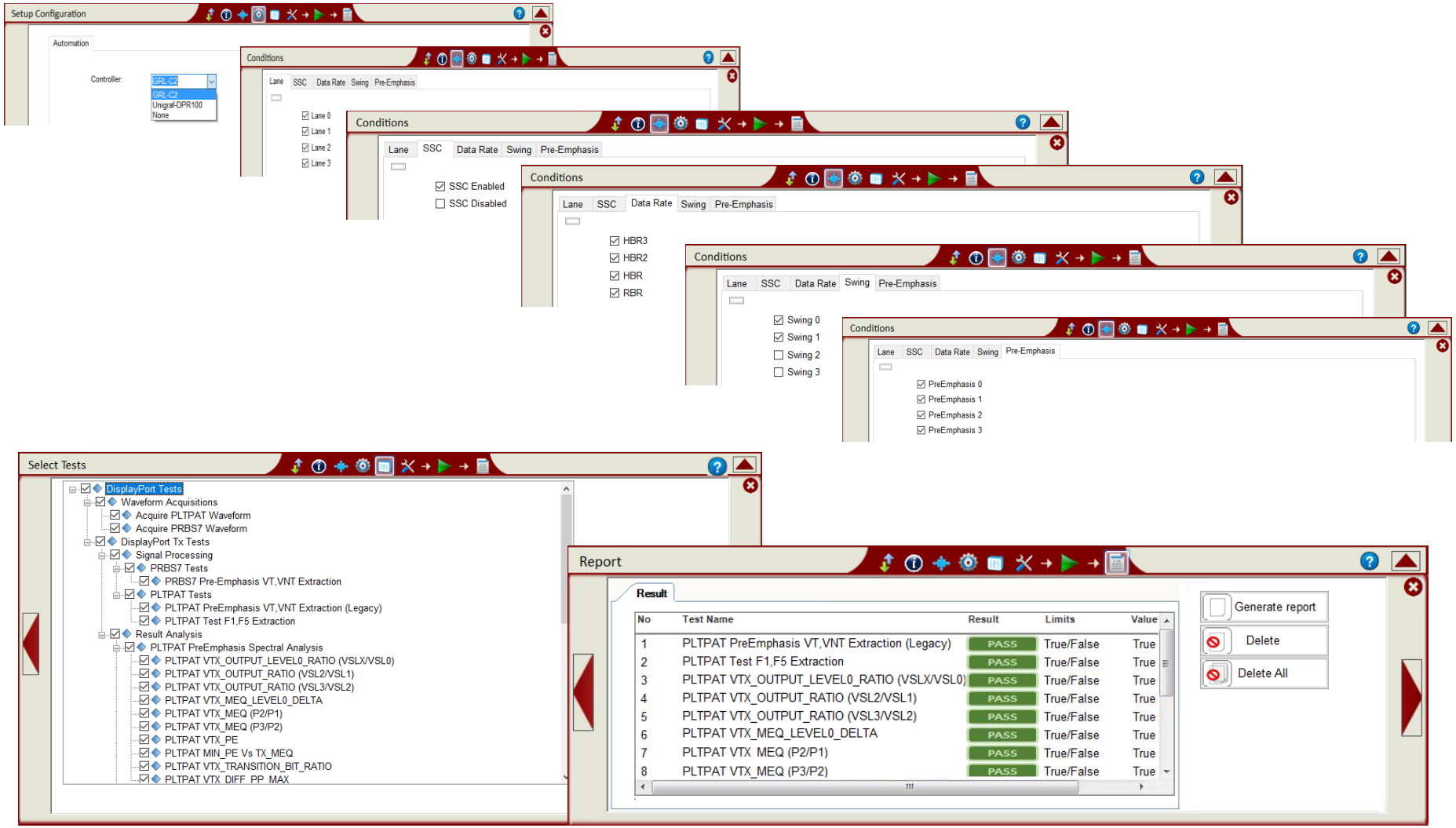
PHY Source Test 2x2 (DP & USB) with USB Crosstalk



For USB-C GRL-USB-PD-C2 Combines Type-C PD Control with DP-AUX Controller to acquire required waveforms 4 Lane Source and 2+2 with xTalk are required by CTS

DP 1.4 HBR3 Source Spectral Test



GRL-DP-Source Software fully Automates Acquisition and Analysis per GRL's approved MOI, uses same framework as GRL Sink SW

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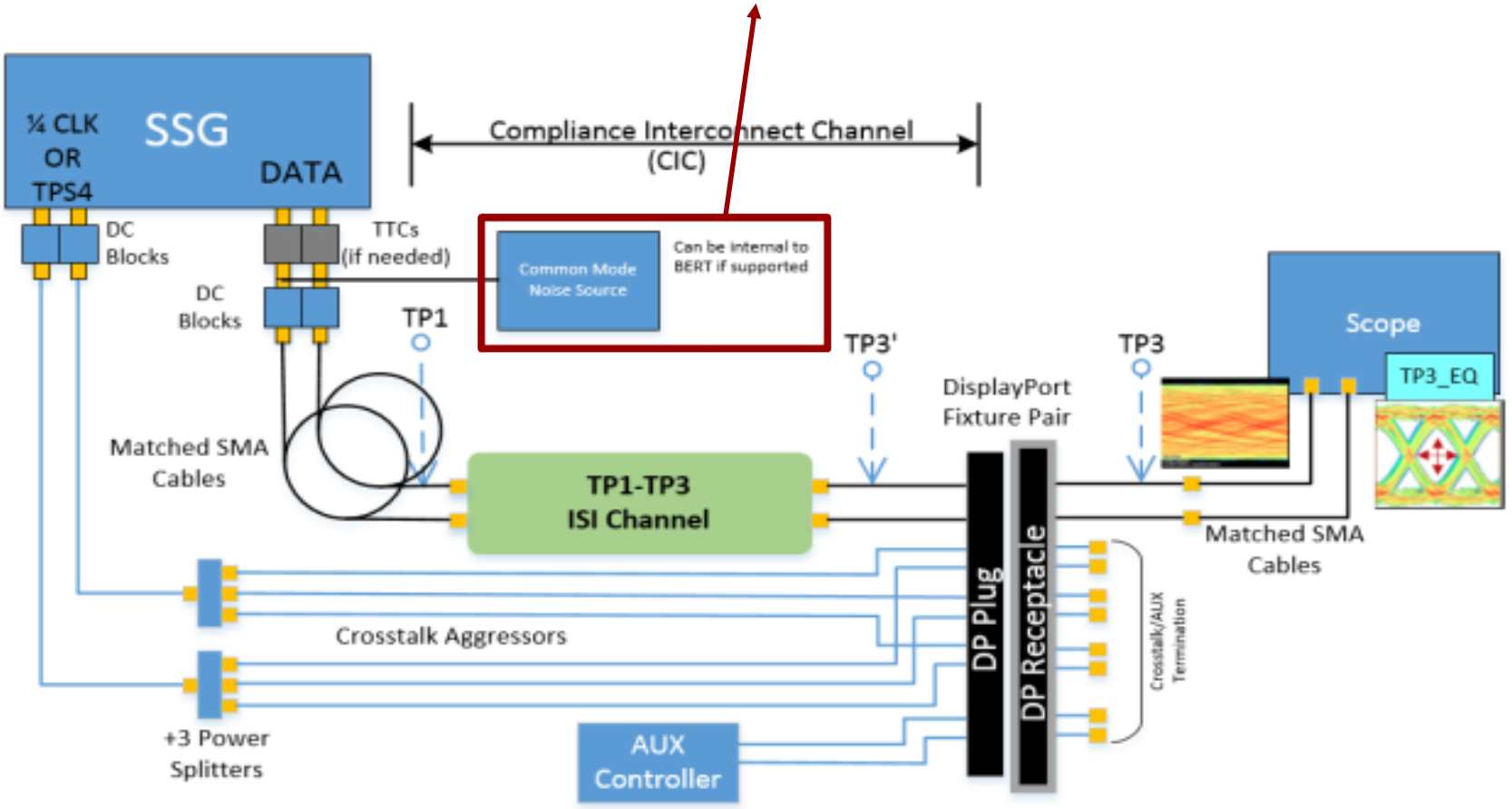
DP 1.4 HBR3 Sink Calibration

For HBR3, Common mode noise of 100 mV_pp @ 400 MHz is injected into the lane under test.



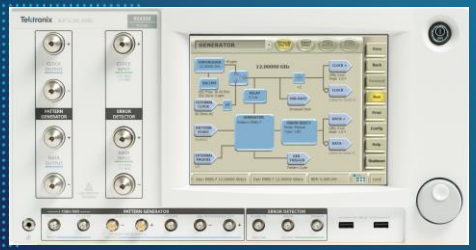
CM Noise is a new Requirement in DP1.4 Sink CTS (Chapter 4 of CTS) – Implemented in Tektronix BSX MOI

DisplayPort 1.4 PHY CTS Source & Sink Test Solutions

Featuring GRL as Development Partner

TekScope SX

BERTScope BSX

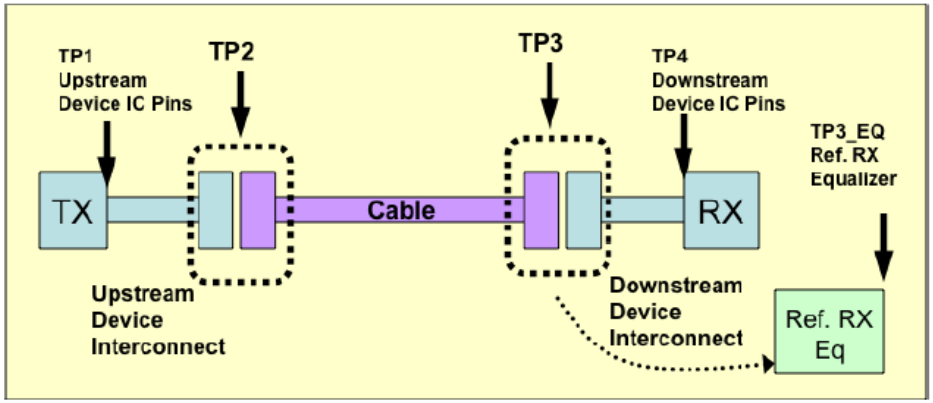


Compliance Test Points

- TP1: at the pins of the transmitter device
- TP2: at the test interface on a test access fixture near end
- TP3: at the test interface on a test access fixture far end
- TP3_EQ: TP3 with equalizer applied
- TP4: at the pins of a receiving device

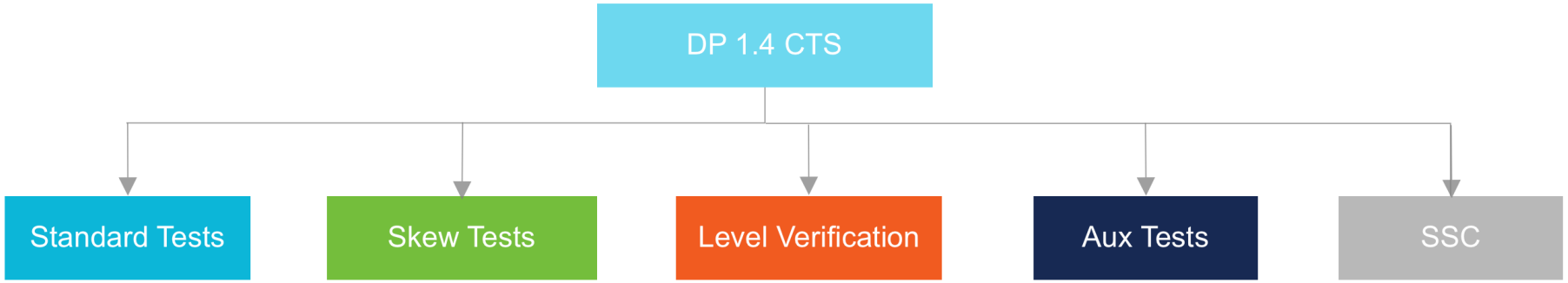
NORMATIVE test points

INFORMATIVE test points



DP 1.4 CTS Fully Defines TP2 as Normative Test Point Used for Tethered Sinks and Adapters

DP1.4 CTS Source (TX) Measurements (Chapter 3)



3.1 Eye-diagram Testing
3.10 AC Common Mode Noise
3.11 Non ISI Jitter Measurements
3.12.1 Total Jitter (TJ) and Deterministic (DJ) Measurements
3.12.2 Random Jitter (RJ) Measurements
3.14 Main Link Frequency Compliance

3.4 Inter Pair Skew Test
3.5 Intra-Pair Skew Test

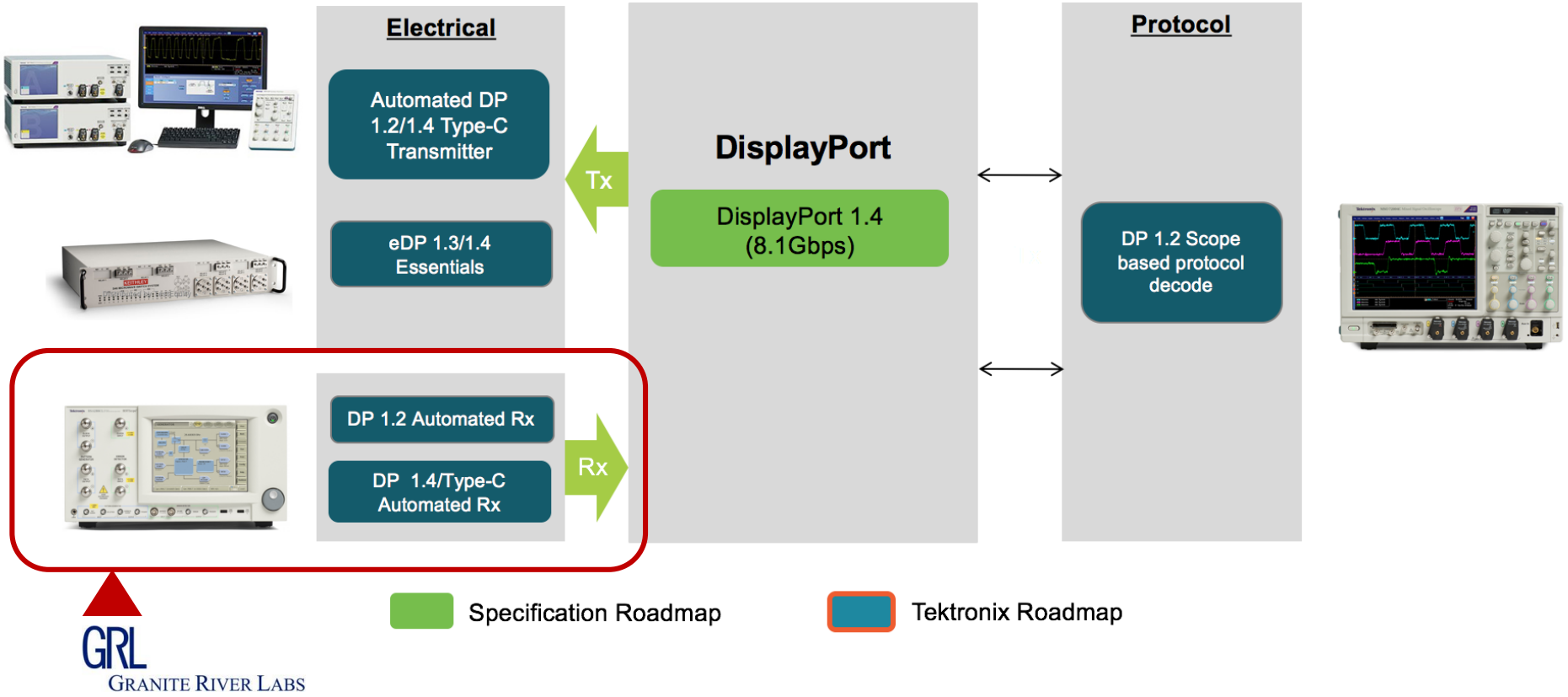
3.2 Non Pre-Emphasis Level Verification Testing
3.3 Pre-Emphasis Level Verification Testing

8.1 AUX Manchester Channel Eye Test
8.2 AUX Manchester Channel Sensitivity Test
8.5 AUX Inrush Test

3.15 Spread Spectrum Modulation Frequency
3.16 Spread Spectrum Modulation Deviation
3.17 dF/dt Spread Spectrum Deviation HF Variation

Full List of Source Measurements to be performed
Performed with Tektronix TekExpress SW

DisplayPort Solutions



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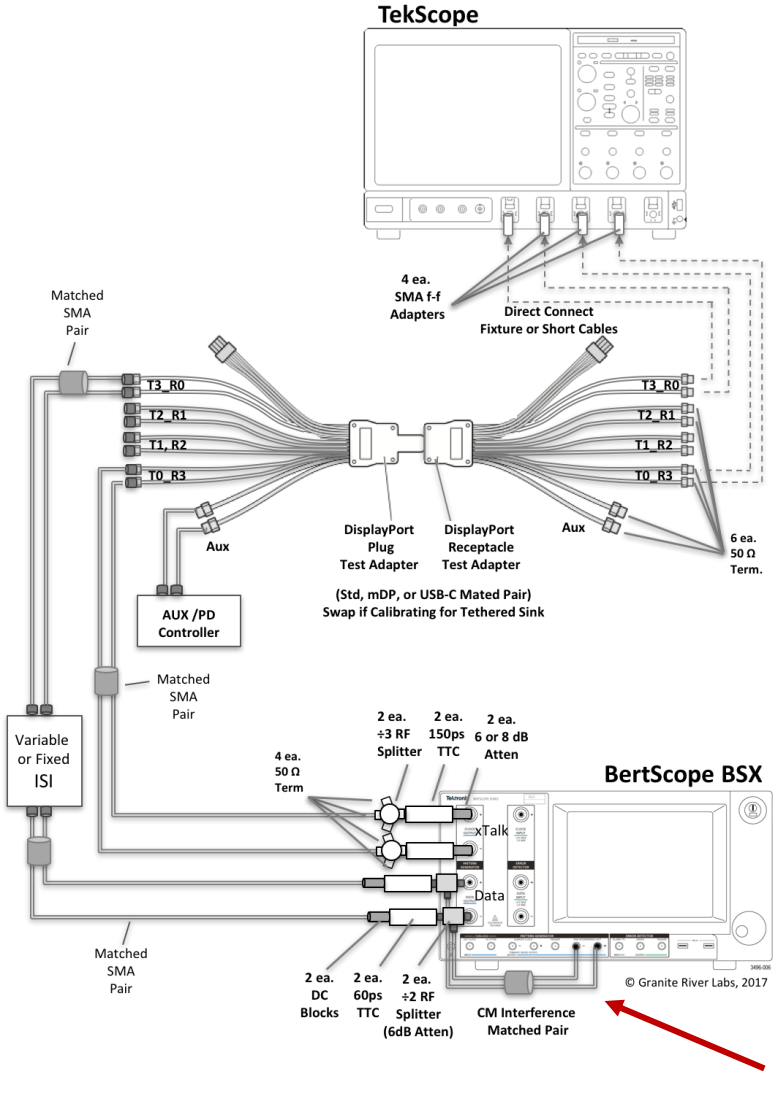
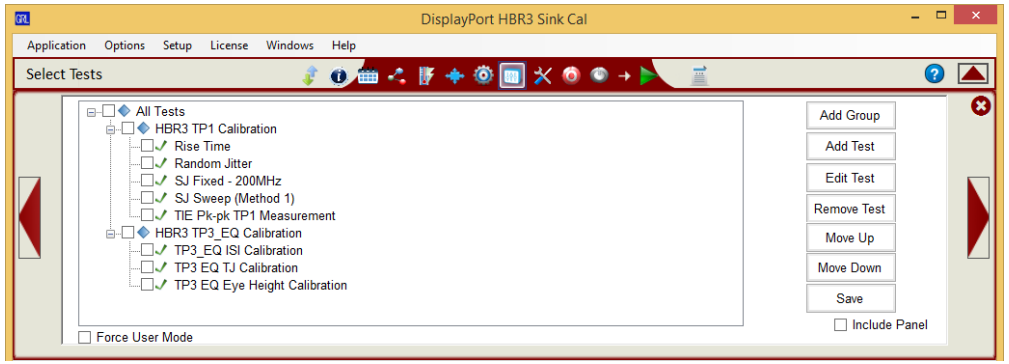
GRL is Development Partner for DP1.4 Sink Test SW for BertScope BSX
MOI has been reviewed and Approved by VESA

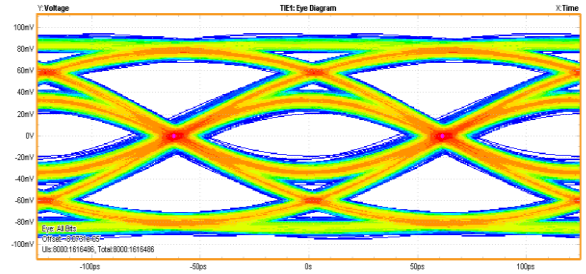
DP1.4 HBR3 PHY CTS Sink Calibration



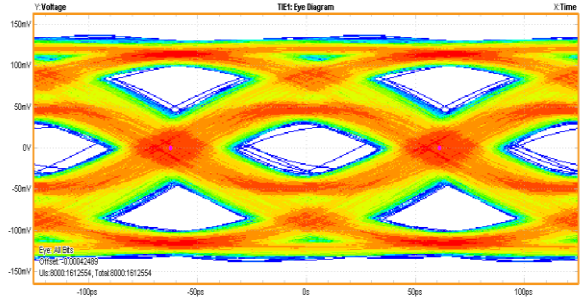
GRL Calibration & Test Software



TP3 ISI Calibration



TP3_CTLE EH Calibration



Setup Shows how CM Noise is Injected
ISI using Artek CLE-1000 tests all data rates with single setup

DP1.4 HBR3 PHY CTS Sink Test

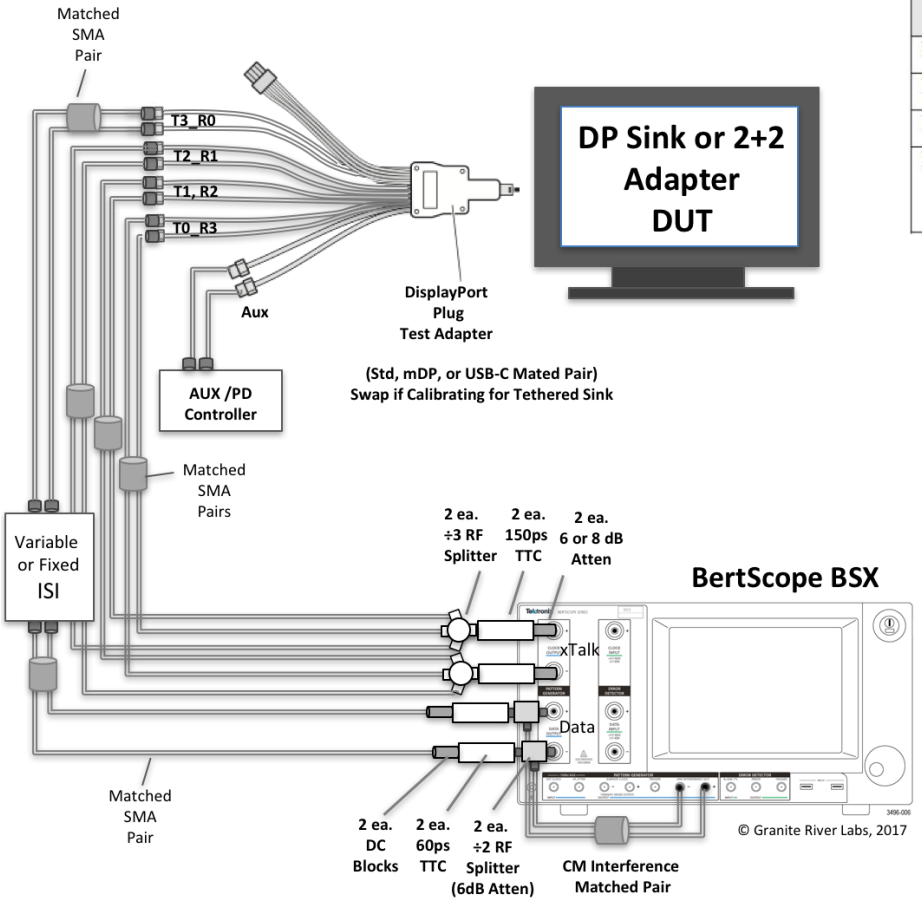


Table 4-52: TP1/TP3 Crosstalk Settings

Data Rate	Aggressor Pattern	TP1/TP3 TTC	TP3 Amplitude (mVp-p)	EH and BER Test Pattern	Comment
RBR	D24.3	NA/150 ps	138	PRBS7	
HBR	D24.3	NA/150 ps	450	PRBS7	
HBR2	D24.3	NA/150 ps	300	CP2520	
HBR3	D24.3	60ps/150 ps	300	TPS4	HBR3 TP1 test 20-80 target is 40ps

Table 4-3: HBR3 TP3_CTLE Jitter Component Settings[a]

Frequency (SJ) (MHz)	TJ (JTHBR3rx) (mUI)	ISI[b] (mUI)	RJ_{RMS} (mUI)	Approximate SJ_{SWEEP} (mUI)	SJ_{FIXED} at 297MHz[c] (mUI)	Crosstalk[d] (mUI)
2	620	240	13	1013	130	20
10				137		
20				109		
100				100		

Table 4-1: BER Measurement Test Parameters

Jitter Frequency (MHz)	Number of Bits	Maximum Number of Allowable Bit Errors	Bit Rate	Observation Time (Seconds)[a]	Data Rate Offset
2	10^{12}	1000	HBR3	123	0
			HBR2	185	
			HBR	370	
			RBR	620	
10	10^{11}	100	HBR3	13	+350ppm
			HBR2	19	
			HBR	37	
			RBR	62	
20	10^{11}	100	HBR3	13	0
			HBR2	19	
			HBR	37	
			RBR	62	
100	10^{11}	100	HBR3	13	0
			HBR2	19	
			HBR	37	

Automated testing performed using DP14-SINK-BSX
And Providing Compliance Report

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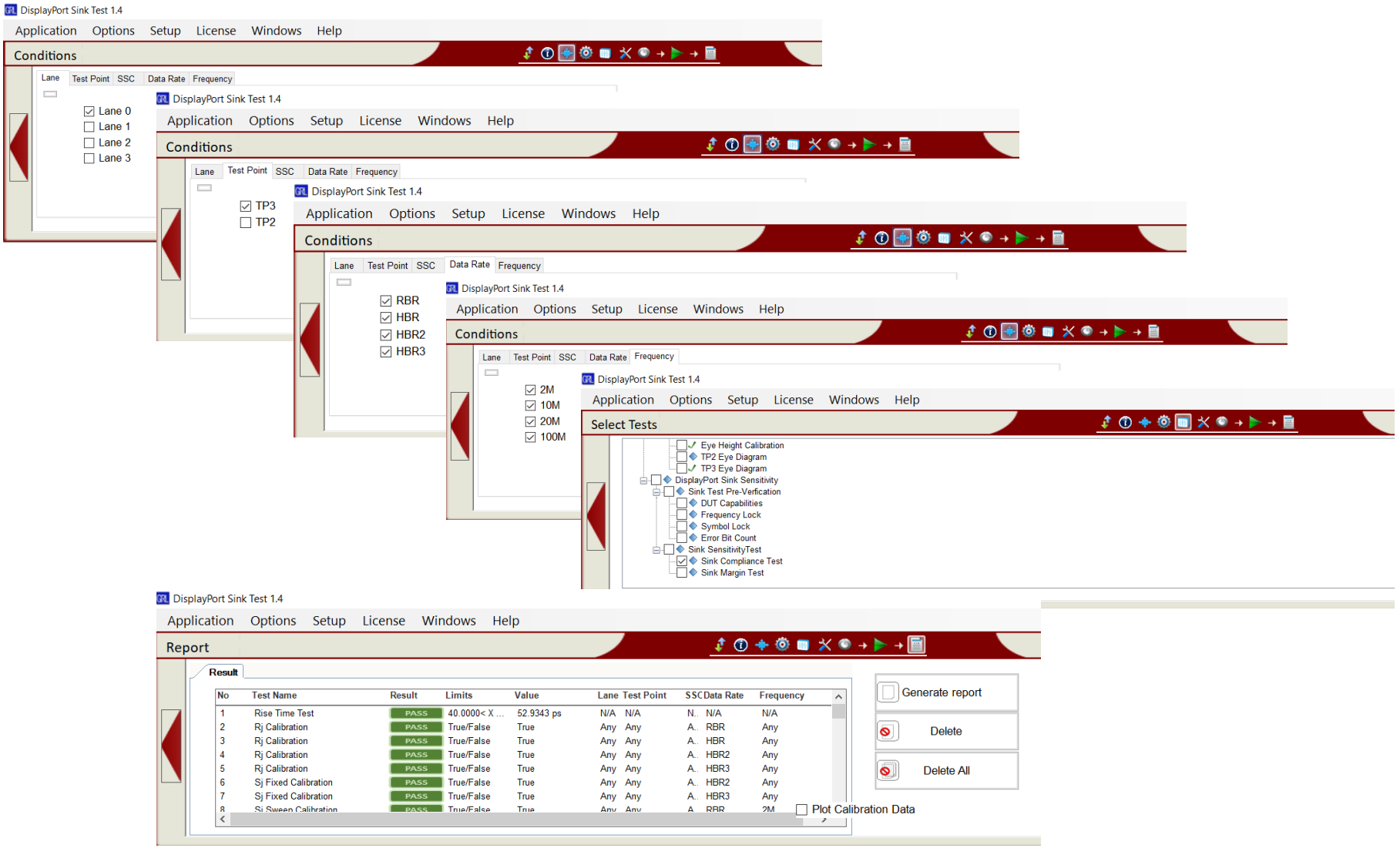
DP1.4 HBR3 PHY CTS Sink Test

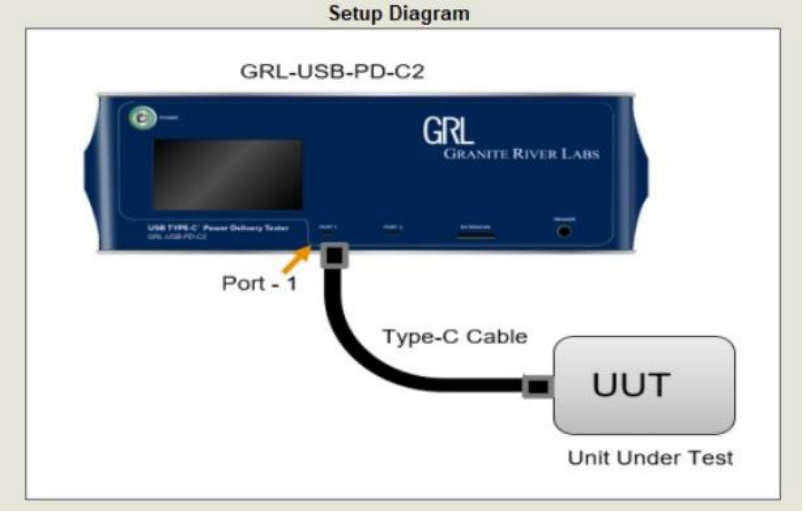


Easy to use intuitive User Interface
Same tools and results as GRL Lab for VESA Logo

VBUS and VCONN Verification

Test Steps

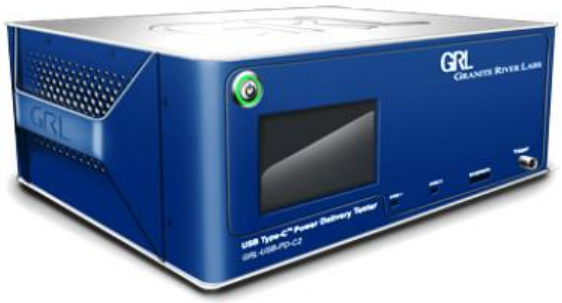
1. Use attached test configuration.
2. Apply 1W load to Vconn and apply load to VBUS.
3. Verify that Voltage value meets USB Type-C Specification limits.
   Pass/Fail1 VBUS = 4.75V to 5.5V
   Pass/Fail2 Vconn = 4.75V to 5.5V
4. Enter DP alt mode.
5. Apply 1.5W load to Vconn and apply load to VBUS.
6. Verify that Voltage value meets DP Alt Mode on USB Type-C Standard requirements.
   Pass/Fail1 VBUS = 4.75V to 5.5V
   Pass/Fail2 Vconn = 2.7V to 5.5V
7. Exit DP alt mode.
8. Apply 1W load to Vconn and apply load to VBUS.
9. Verify that Voltage value meets USB Type-C Specification limits.
   Pass/Fail1 VBUS = 4.75V to 5.5V
   Pass/Fail2 Vconn = 4.75V to 5.5V



GRL DisplayPort Test Solutions

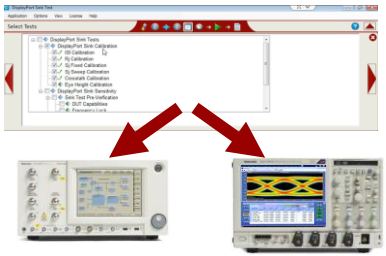
- **GRL-USB-PD-C2 - USB Type-C™ and USB Power Delivery Compliance Tester & Analyzer**
  - PHY Test Automation for DP-C, TBT3, USB Type-C
  - USB PD Tests for DP-C Compliance **(Chap 10 &11)**
  - USB PD 3.0/2.0 and Quick Charge 4

  … and much more



- **Source Tx PHY Test Automation for Multi-vendor Oscilloscope. (GRL-DP14-SOURCE)**
  - DP source spectral and pre-emphasis level testing.
  - Automatically acquire/analyze waveform for the testing.

- **Sink PHY Test Automation for the Tektronix BERTScope (GRL-DP14-SINK)**
  - Automatically calibrates BERT and Scope to create stressed eye for Sink Jitter Tolerance testing
  - 1.4 Draft and 1.2 CTS



BERTScope Tek Scope

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Tektronix Solutions Partner

Various Products can get DP logo by GRL

DPC Monitor

DPC C to DP adapter (cable)

DPC Desktop/NB

Certified products tested by GRL

DPC Converter

DPC External Docking

DPC Multi-adapter

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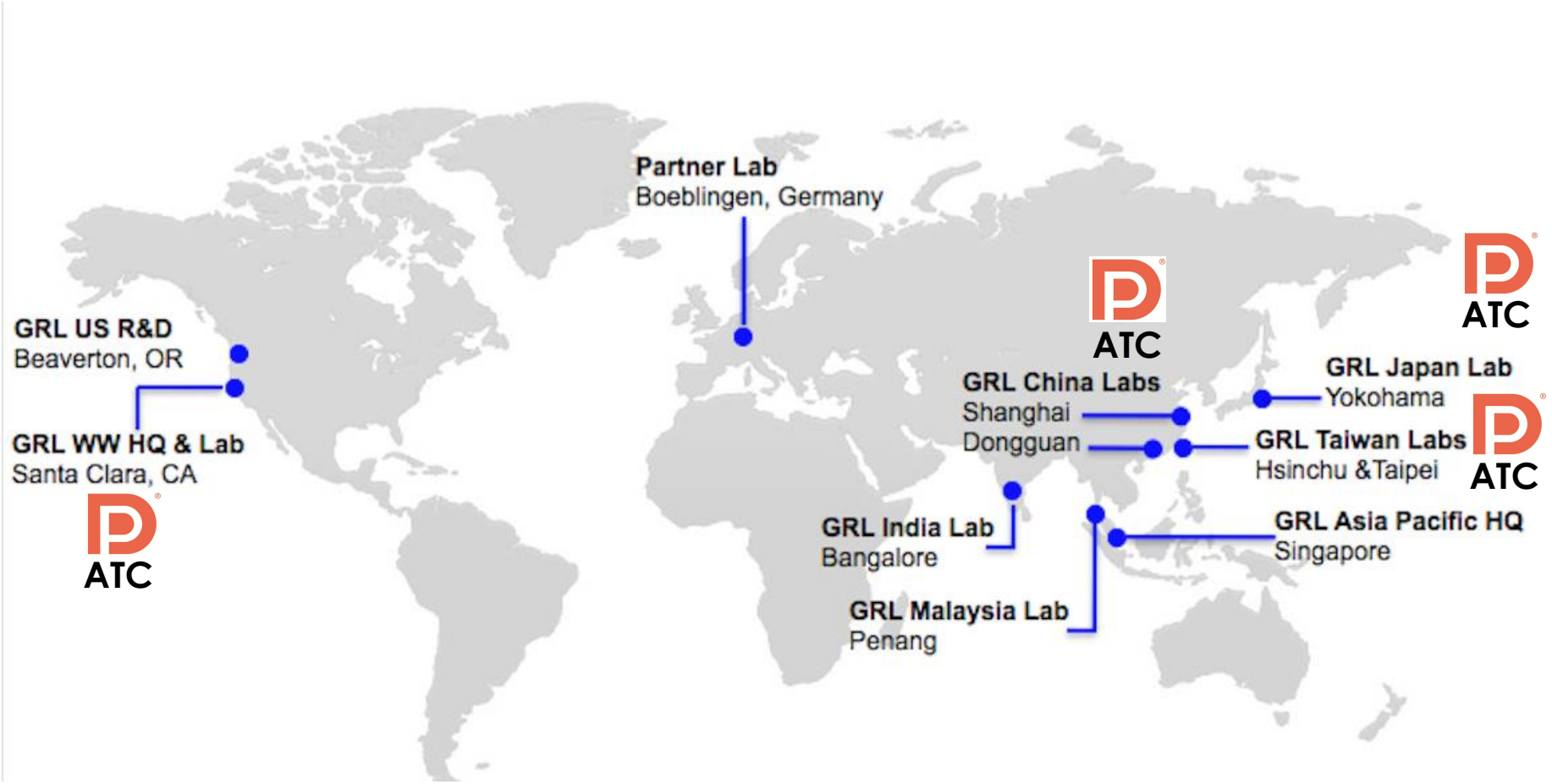
GRL Convenient Locations

4 DisplayPort ATCs, Shanghai is new test Lab of DPATC



Thank You

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