

**GRL**

GRANITE RIVER LABS



## GRL's Experience with DisplayPort Over USB Type-C Testing

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# Agenda

- GRL Introduction
- Approach to the USB Type-C Ecosystem(s)
- Support of DisplayPort Over Type-C Test Program
- GRL Solutions Developed for USB Type-C
- Summary

# Connectivity Standards Covered



Authorized Test Lab

## Data Bus & Storage

## High Definition Video

 <b>THUNDERBOLT</b> ATC 20G	 <b>FCIA</b> 16/32G	 <b>SERIAL ATA</b> ATC Express
 <b>PCI EXPRESS</b> PCIe Gen3/4	 Serial Attached SCSI SAS Gen3/4	 <b>SUPER SPEED USB</b> ATC 10G

 <b>SlimPort</b> ATC Type C	 <b>DisplayPort</b> ATC eDP/DP 1.3	 <b>SMPTE</b> 3G/HD-SDI
 <b>MHL</b> ATC MHL 3 Future	 <b>HDMI</b> ATC HDMI 1.4/2.0	 <b>V-by-One</b> V-By-One HS

 <b>INFINIBAND</b> SDR DDR QDR FDR EDR	 <b>IEEE 802</b> 10G-BaseT 100/400G SFI-SFP+ QSFP28 CAUI-4	 <b>ITU</b> SONET STM-16 STM-64 ODU-2
	 <b>OIF</b> CEI 25/28G	

 <b>OPEN INTERCONNECT</b> OIC
 <b>THREAD</b> Thread

 <b>USB</b> ATC Type C/PD
 <b>MIPI</b> D-PHY/M-PHY

 <b>UFS</b> ATC UFS Future
 <b>SD</b> ATC UHS-2

 <b>CFA</b> CompactFlash Association ATC CFast, XQD
 <b>JEDEC</b> DDR3/eMMC

## Datacom & Telecom

## IOT

## Mobile

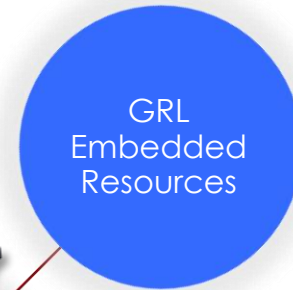
## Memory Bus & Card

# GRL Customer Engagement Models



## Customer uses GRL Lab to augment Internal resources

- Convenient lab locations
- Full access to test experts
- Full access to golden test environments



## GRL places test resources and methodology at customer site

- Engineering contractors
- Turnkey golden test environment replication
- Convenient in-house testing

## Customer uses GRL solutions in R&D lab or factory

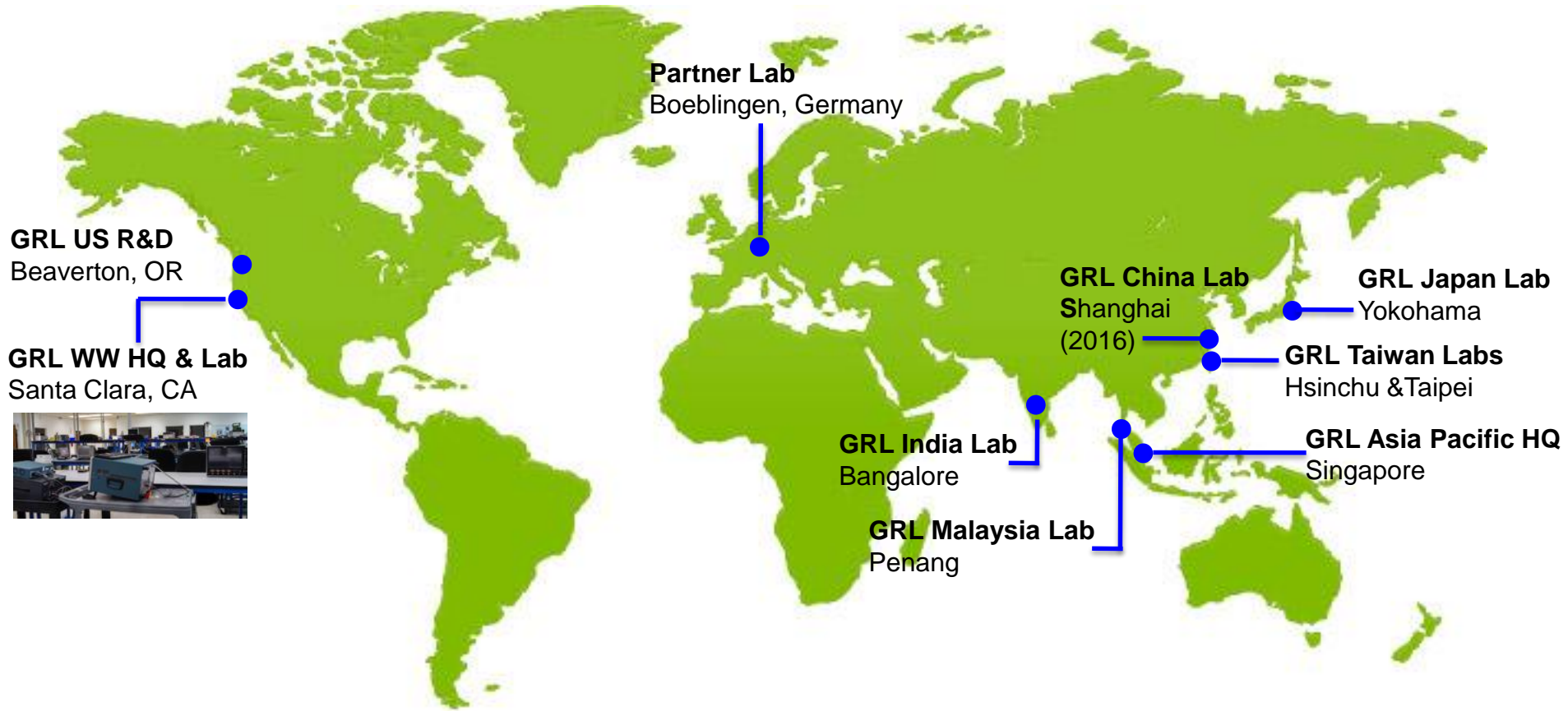
- Execute CTS tests with easy to use approved solutions
- Flexible test coverage from simple functional checks to deep multilayer stress testing



## Customer sends DUT for official certification to GRL

- Many standards supported
- Work with customer to debug and pass compliance
- First to offer compliance for new standards

# GRL Convenient Locations

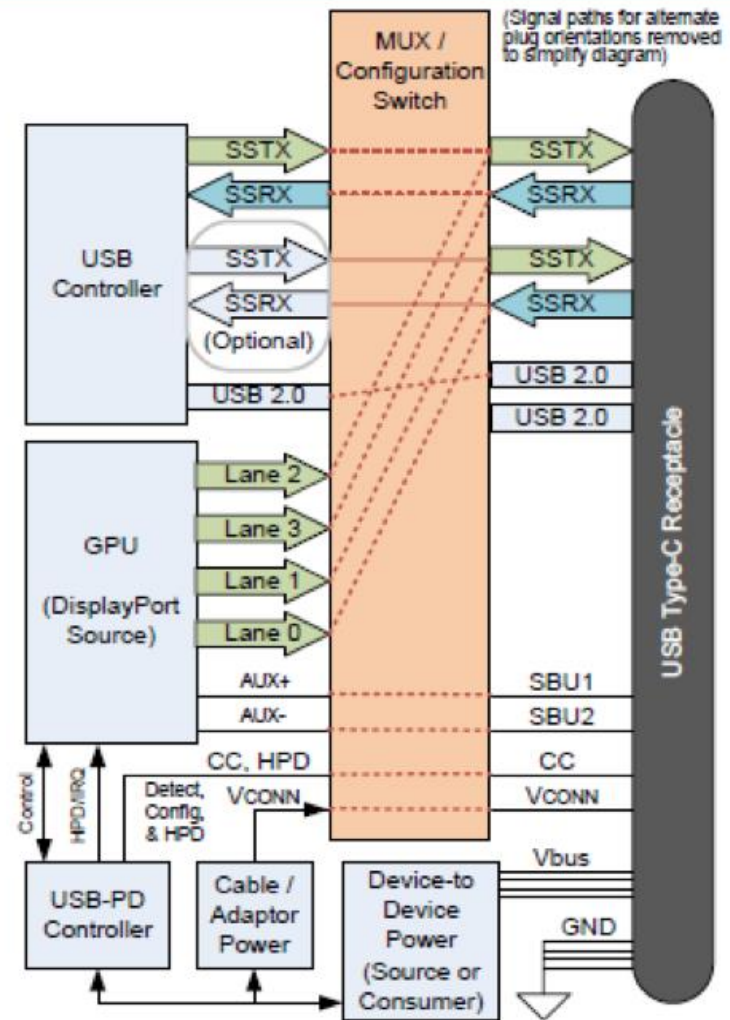
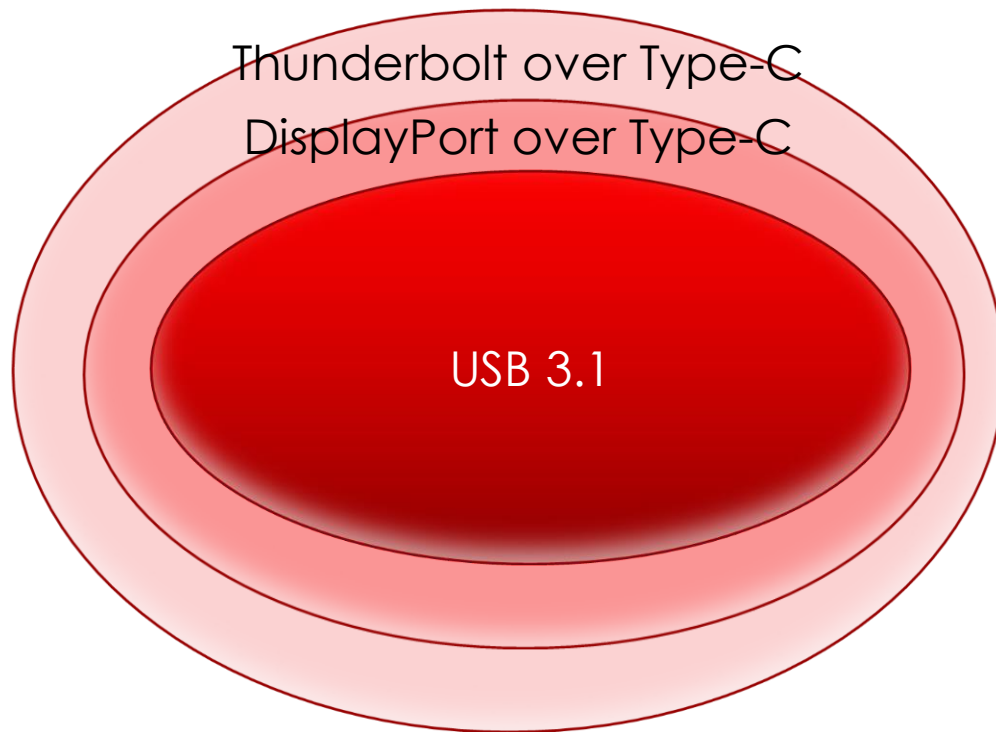




# USB Type-C Product Trend



# USB Type-C Simple User Experience... Complex System Needs Testing



# GRL's Core Competencies



- 20 Years of Test Methodology and Test Solution Development
- Authorized Test Center for High Speed Standards
  - USB2.0/3.0 Device, Host, Hub – (Santa Clara, Taiwan, **Japan**)
    - **Bangalore, India (mid-2016)**
  - DisplayPort – (All locations)
  - Thunderbolt – (Santa Clara, Taiwan)
  - MHL/HDMI – (Taiwan, India)
  - SATA – (All locations)...
- GRL is member of all applicable WGs in USB (and VESA)
  - USB PD
  - USB Newark
  - USB Dublin
  - USB 3.1 PHY CTS
  - VESA DisplayPort over Type-C ...



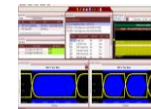
# GRL's Approach to Ecosystem(s)



- Follow Industry Group Timelines for Lab Certification
  - USB – Pre-Certification of Hosts/Devices – Official: Late 2016
  - DisplayPort – Support VESA Early 'Best Effort' Logo Program
  - Thunderbolt – Approved for Host Certification Testing
- Use Current Best Known Practices for Testing
- Supplement existing CTS Drafts with Custom CTS Development
- Pretesting Available 24/7 for Customer Testing in all locations
  - Santa Clara, Taiwan, India, Japan
  - Not Limited to IOP or USB Workshop Timing
- Support Multiple Vendor TE Solutions where they exist

**GRL-USB-PD  
Solution**

■ Develop TE Solutions where needed



- Partner with other Ecosystem TE vendors and labs as needed
  - Example: ETC for Cables and Connectors

# DPC Host test plan (Best Effort)



1. USB Type C test items
  - a. USB PD tests => BMC Phy, Protocol  
Customer shall provide USB-PD .txt file
  - b. USB 3.0 => Electrical Tx / Rx , LFPS  
Customer shall enable USB 3.0 PHY Compliance Test Patterns
  - c. USB 2.0 => Electrical
  - d. USB link layer tests
  - e. USB 3.0 Gold tree Interop Tests
  
2. Displayport over USB Type C test items
  - a. DPC source PHY test => main link , AUX eye
  - b. DPC source Link layer Testing
  - c. DPC Interop Testing
  - d. DPC MST test if support  
Customer shall provide DisplayPort PHY (CDF)  
Customer shall provide tools for PHY Settings  
(Pattern, Level, Pre-Emphasis)



# DPC Adapter test plan (Best Effort)



1. USB Type C test items
  - a. USB Power Delivery tests => BMC Phy, Protocol  
Customer shall provide USB-PD .txt file
  - b. USB 3.0 => Electrical Tx / Rx , LFPS if support USB 3.0  
Customer shall enable USB 3.0 PHY Compliance Test Patterns
  - c. USB 3.0 Gold tree Interop Tests if support 3.0
  - d. USB CV tests if support 3.0
  
2. Displayport over USB Type C test items
  - a. DPC sink PHY test => main link , AUX eye
  - b. DPC sink Link layer Testing
  - c. DPC Interop Testing  
Customer shall provide DisplayPort PHY (CDF)  
Customer shall provide tools for PHY Settings  
(Pattern, Level, Pre-Emphasis)





# Issues Found During Testing

GRL has already tested many early market DP Over Type-C Products and have Certified a few. Most common Issues found are...

- USB Type-C Functional Test Failures
- USB Power Delivery (BMC Eye, Protocol, Power Provider/Consumer) Test Failures
- DisplayPort Specific Failures (Case Study Included)
  - Host Failures of AUX DC Test
  - Host Link Failures on IRQ
  - Sink with Power Charging Doesn't light up with Chromebook

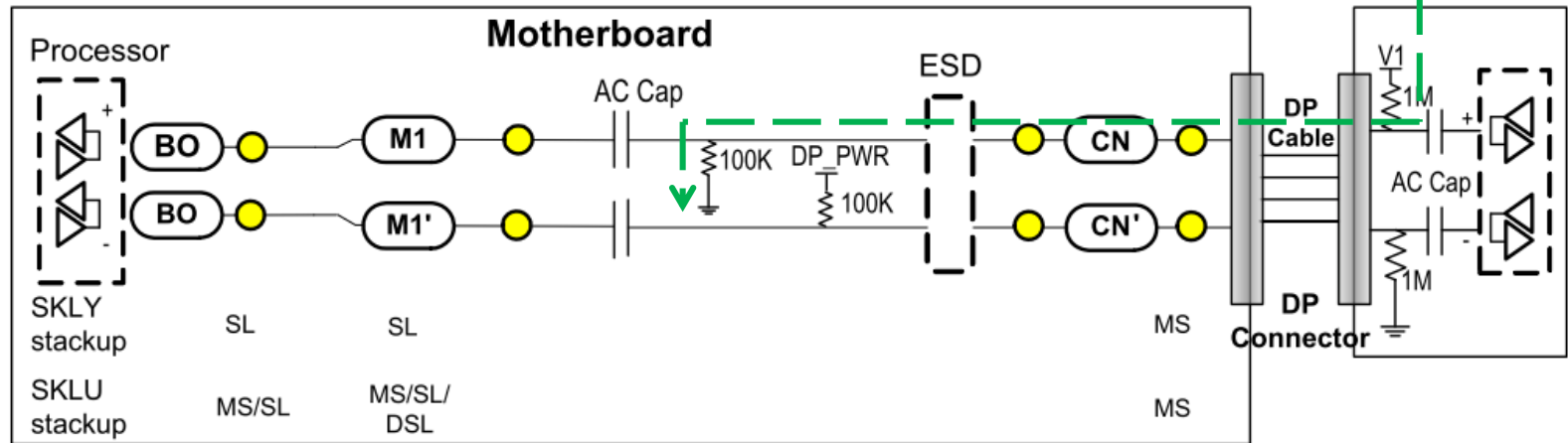
# Common issue one : DPC Host fail on AUX Channel DC Test: AUX+ Termination Power Off

■ DP CTS test 8.4 AUX Channel DC Test : AUX+ Termination fail in type-c port. The voltage of AUX+ always be keep in 0.5V

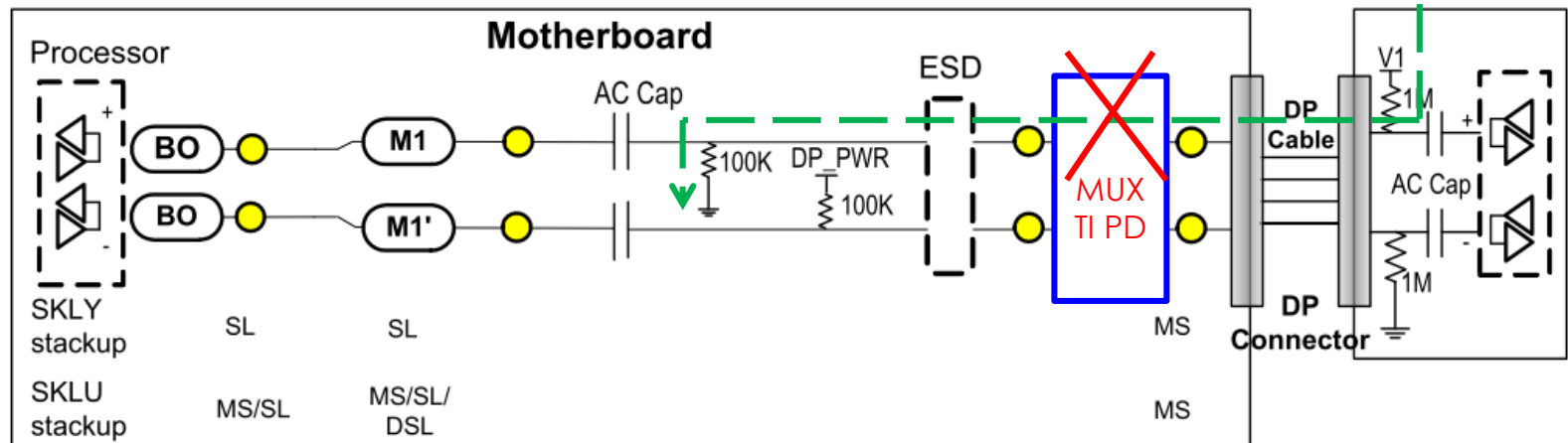
➤ Measurement Requirements :

- Create a voltage divider on AUX+ by a resistance, R2 (1M $\Omega$ ) to a termination voltage of 3.3 V DC ( $\pm$  5%). Measure V [AUX+] with a DC voltmeter. Test is made with DUT powered on and DUT powered off.
- 0.0 V DC  $\leq$  V [AUX+]  $\leq$  0.4 V DC .

➤ Standard AUX Channel Topology



➤ Type-C AUX Channel Topology : add MUX (TI PD) between pull up/down resistor and connector for flip mode.





# Common issue two : DPC Host link layer fail on IRQ

## TEST SUMMARY

TEST	PASSED	FAILED	TIMED OUT	SKIPPED
22 - (4.3.2.1) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Symbol Lock	0	2	0	0
23 - (4.3.2.2) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Clock Recovery Lock	0	2	0	0
24 - (4.3.2.3) Successful Link Re-training After IRQ HPD Pulse Due to Loss of Inter-lane Alignment Lock	0	2	0	0

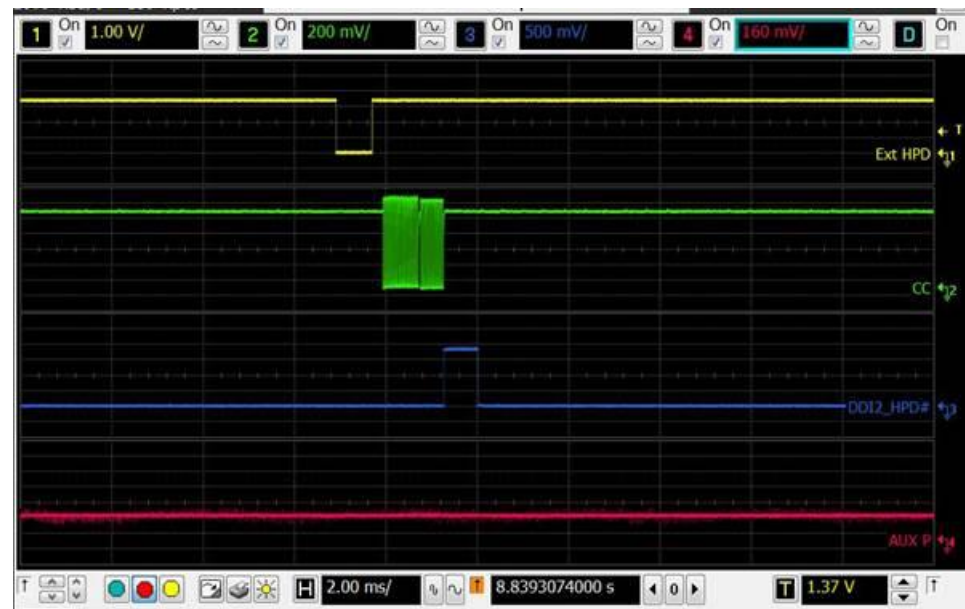
Mostly the problem is the PD controller handle IRQ timing not well, so make the IO pin to GPU didn't action right. So GPU didn't read the DPCD again.



We connect the DPR 100-> Dongle-> DUT.

- CH1 : DPR100 HDP
- CH2 : Dongle CC
- CH3 : DDI2\_HPDP (After PD controller)
- CH4 : Aux positive. You can see the HPD IRQ

The DPR100 can transfer as CC regenerate from PD controller within 2ms. But the GPU didn't read the DPCD from Aux. So, the fail is GPU didn't take action when he saw the IRQ from PD controller.



## Common issue three :

# DPC sink with power charging can't light up with Chrome pixel



- Some DPC sinks can't light up by Chrome pixel and PD keep reset again then again.
- Because the sink standd by limit is 500mW and Chrome pixel seems over spec.

### USB Type-C & PD Spec Overview

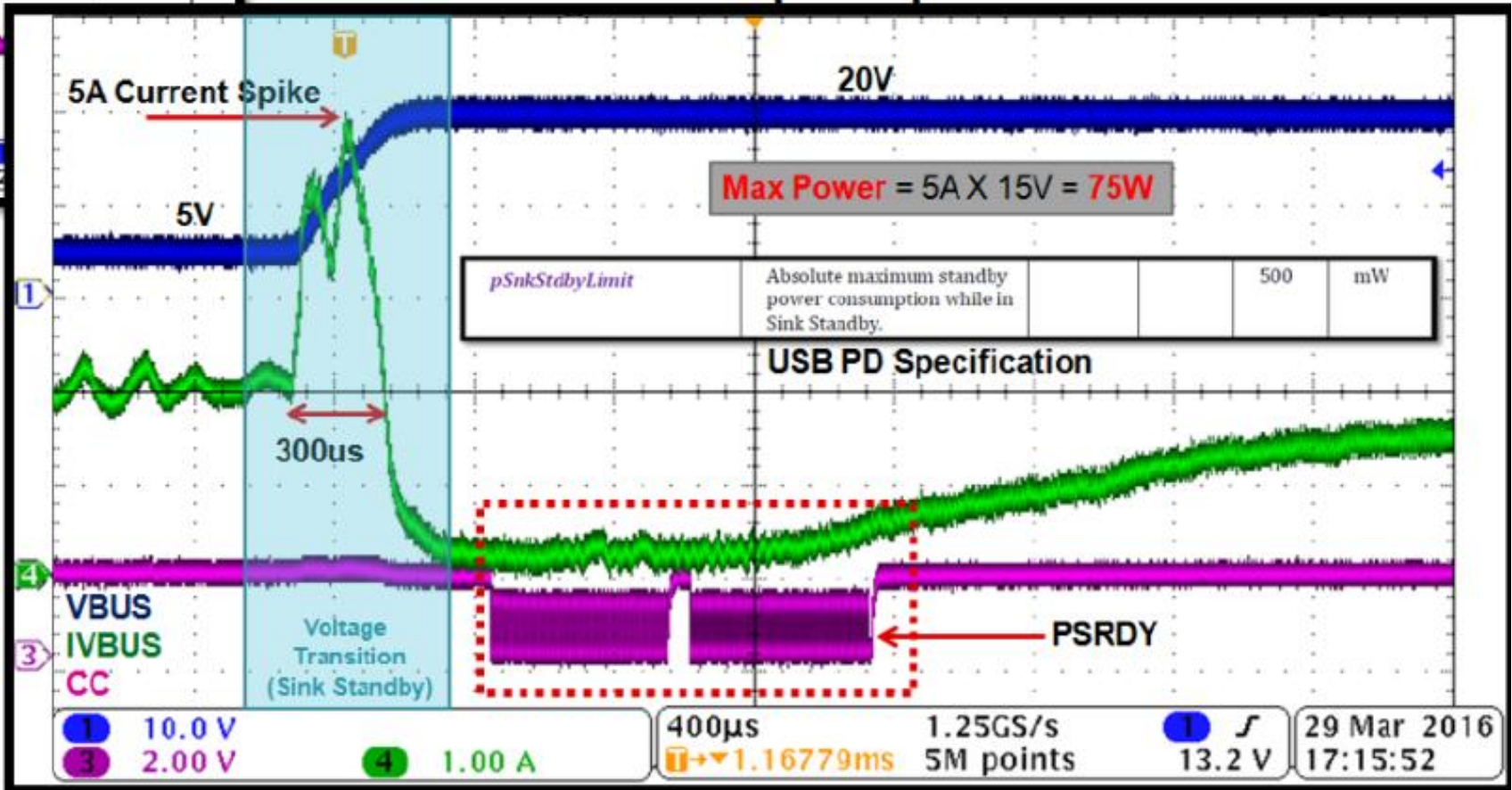
- The USB PD specification has specific power consumption for transitions
  - Helps prevent brown out conditions on power adapters and/or charging devices
  - High current spikes may damage discrete Power FETs during voltage transitions
- A Sink of power must not draw more than the absolute 500mW max during a transition
- Notebook design consideration must be taken into account
  - Proper design and configuration of battery charger

7.2.3 Sink Standby						
The Sink shall transition to Sink Standby before a positive or negative voltage transition of $V_{BUS}$ . During Sink Standby the Sink shall reduce its average power draw to $pSnkStdby$ and its peak power draw shall not exceed $pSnkStdbyLimit$ . This allows the Source to manage the voltage transition as well as supply sufficient operating current to the Sink to maintain PD operation during the transition. The Sink shall complete this transition to Sink Standby within $tSnkStdby$ after evaluating the <i>Accept</i> Message from the Source. The transition when returning to Sink operation from Sink Standby shall be completed within $tSnkNewPower$ . The $pSnkStdby$ requirement shall only apply if the Sink power draw is higher than this level.						
$pSnkStdby$	Average power consumption over a 10ms interval while in Sink Standby.			150	mW	Section 7.2.3
$pSnkStdbyLimit$	Absolute maximum standby power consumption while in Sink Standby.			500	mW	Section 7.2.3

### USB PD Specification



# Zoom In Scope Capture





# GRL's USB Type-C Test Solution

- Tests to Rev1.0 of the USB Power Delivery Test Plan
- Test Controller can be used as an 'Alt Mode Initiator' for DisplayPort PHY Testing

# Introducing GRL USB-PD Compliance Test Solution!



## ■ GRL-USB-PD Software

- *GRL USB-PD Power Delivery Compliance Software*
  - *Runs on multiple Vendor's Windows Based Oscilloscopes!*
  - *Performs BMC-PHY Tests*
  - *Decodes USB-DP Protocol*
  - *Automates Compliance Tests when used with Type-C Test Controller*

**New!!**

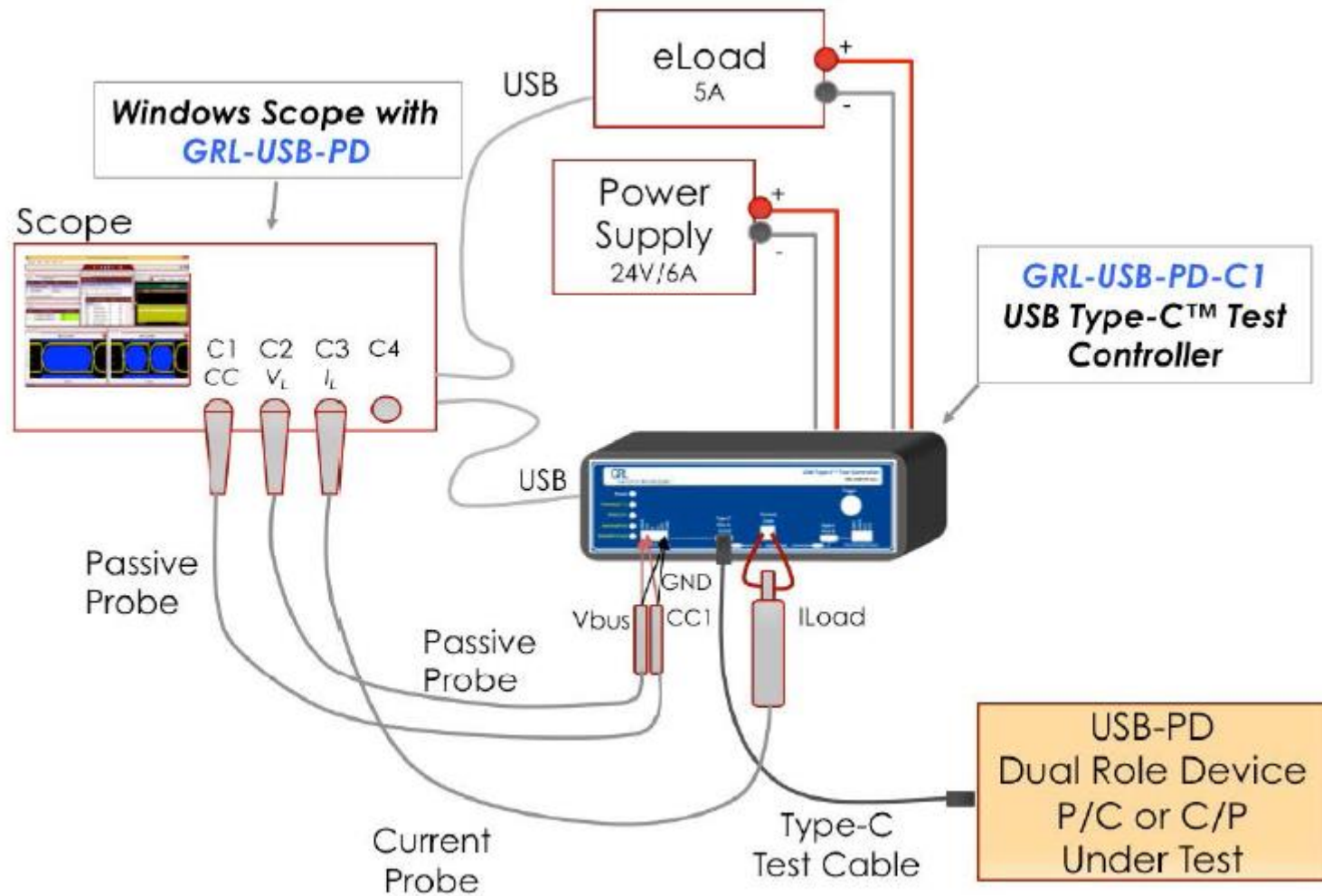
## ■ GRL-USB-PD-C1 Hardware

- *GRL Type-C Test Controller*
  - *Transforms Oscilloscope into USB-PD Compliance Tester!*





# Power Delivery Test Setup





# USB-PD Device Compliance Tests



## Primary Tests

Test Ref #	Test Name	Test Description	Required Tests by Device Type					
			DRP	Provider Only	Consumer Only	Dual Role Device		
						C/P	P/C	
		<b>Primary Power Delivery Device Tests</b>						
		<b>BMC PHYSICAL LAYER TESTS - TRANSMIT</b>						
TDA.2.1.1.1	BMC-PHY-TX-EYE	BMC Transmitter Eye Diagram Test		✓	✓	✓	✓	✓
TDA.2.1.1.2	BMC-PHY-TX-BIT	BMC Transmit Bit Rate and Bit Rate Drift		✓	✓	✓	✓	✓
		<b>BMC PHYSICAL LAYER TESTS - RECEIVE</b>						
TDA.2.1.2.1	BMC-PHY-RX-BUSIDL	BMC Bus Idle Detection Test		✓	✓	✓	✓	✓
TDA.2.1.2.2	BMC-PHY-RX-INT-REJ	BMC Receive Interference Rejection Test		✓	✓	✓	✓	✓
		<b>BMC PHYSICAL LAYER TESTS - MISCELLANEOUS</b>						
TDA.2.1.3.1	BMC-PHY-TERM	BMC Termination Impedance Test		✓	✓	✓	✓	✓
TDA.2.1.3.2	BMC-PHY-MSG	BMC PHY Level Message Test		✓	✓	✓	✓	✓
		<b>PROTOCOL SPECIFIC - Message Checks</b>						
TDA.2.2.1	BMC-PROT-SEQ-GETCAPS	Get_Source_Cap and Get_Sink_Cap Test	✓	✓	✓	✓	✓	✓
TDA.2.2.2.1	BMC-PROT-SEQ-CHKCAB-P-PC	Check Cable Capabilities (3A Marked) Test	✓	✓				✓
TDA.2.2.2.2	BMC-PROT-SEQ-CHKCAB-NOMRK-P-PC	Check Cable Capabilities (Unmarked) Test	✓	✓				✓
TDA.2.2.2.3	BMC-PROT-SEQ-CHKCAB-CP-ACC	Check Cable Capabilities (3A Marked) Test - After PR Swap	✓				✓	
TDA.2.2.2.4	BMC-PROT-SEQ-CHKCAB-NOMRK-CP-ACC	Check Cable Capabilities (Unmarked) Test - After PR Swap	✓				✓	
TDA.2.2.3	BMC-PROT-SEQ-DRSWAP	Dual Role Swap Test	✓	✓	✓	✓	✓	✓
TDA.2.2.4	BMC-PROT-SEQ-VCSWAP	VCONN Swap Test	✓	✓	✓	✓	✓	✓
TDA.2.2.5	BMC-PROT-DISCOV	ID Checks	✓		✓	✓	✓	
TDA.2.2.6	PROT-SEQ-SWAP-REJ	Reject Swap Test - Provider/Consumer	✓					✓
TDA.2.2.7	BMC-PROT-BIST-NOT-5V-SRC	BIST Functionality at Above 5V Test	>5V DUT Only	>5V DUT Only				>5V DUT Only
TDA.2.2.8	BMC-PROT-REV-NUM	Revision Number Test	✓	✓	✓	✓	✓	✓
		<b>Power Source/Sink Tests</b>						
TDA.2.3.1.1	BMC-POW-SRC-LOAD-P-PC	Source Dynamic Load Test, Provider or Provider/Consumer	✓	✓				✓
TDA.2.3.1.2	BMC-POW-SRC-LOAD-CP-ACC	Source Dynamic Load Test, Consumer/Provider Accepting Swap	✓				✓	
TDA.2.3.2.1	BMC-POW-SRC-TRANS-P-PC	PDO Transition Test - Source, Provider or Provider/Consumer	✓	✓				✓
TDA.2.3.2.2	BMC-POW-SRC-TRANS-CP-ACC	PDO Transition Test - Source, Consumer/Provider Accepting Swap	✓				✓	
TDA.2.3.3.1	BMC-POW-SNK-TRANS-C-CP	PDO Transition, Current Draw and Suspend Test - Sink, Consumer or	✓		✓		✓	
TDA.2.3.3.1	BMC-POW-SNK-TRANS-PC	PDO Transition, Current Draw, and Suspend Test, Sink, Provider/Consumer	✓					✓

Source: USB-PD Test Plan Rev 1.0

# USB-PD Device Compliance Tests

## Secondary Checks



Test Ref #	Test Name	Test Description	Required Tests by Device Type					
			DRP	Provider	Consumer	Dual Role Device		
						C/P	P/C	
		<b>Secondary Tests for all Devices</b>						
		<b>Secondary Message Checks</b> Performed whenever the Appropriat Message is Detected						
TDB.1.1.1	PHY-MSG-GEN	PHY Level General Message Test (SOP*)						
TDB.2.1.2.1	PROT-MSG-HDR	Message Header Checks - Except GoodCRC	✓	✓	✓	✓	✓	✓
TDB.2.1.2.2	PROT-MSG-HDR-GCRC	Message Header Checks - GoodCRC	✓	✓	✓	✓	✓	✓
TDB.2.1.3	PROT-MSG-CTRL	Control Message Checks	✓	✓	✓	✓	✓	✓
TDB.2.1.3.1	PROT-MSG-CTRL-PING	Ping Checks	✓	✓	✓	✓	✓	✓
TDB.2.1.4.1.1	PROT-MSG-DATA-SRC-CAP	Source Capability Message Checks	✓	✓		✓	✓	✓
TDB.2.1.4.1.2	PROT-MSG-DATA-SNK-CAP	Sink Capability Message Checks	✓		✓	✓	✓	✓
TDB.2.1.4.2	PROT-MSG-DATA-REQ	Request Message Checks	✓		✓	✓	✓	✓
TDB.2.1.4.3	PROT-MSG-DATA-VEND	Vendor Defined Message Checks	✓	✓	✓	✓	✓	✓
TDB.2.1.4.4.1.1	PROT-MSG-DATA-VDM-ID-INIT	Discover ID Initiator Message Checks	✓	✓	✓	✓	✓	✓
TDB.2.1.4.4.1.2	PROT-MSG-DATA-VDM-ID-ACK	Discover ID ACK Message Checks	✓	✓	✓	✓	✓	✓
TDB.2.1.4.4.2.1	PROT-MSG-DATA-VDM-SVID-INIT	Discover SVIDs Initiator Message Checks	✓	✓	✓	✓	✓	✓
TDB.2.1.4.4.2.2	PROT-MSG-DATA-VDM-SVID-ACK	Discover SVIDs ACK Message Checks	✓	✓	✓	✓	✓	✓
TDB.2.1.4.4.3.1	PROT-MSG-DATA-VDM-MODE-INIT	Discover Modes Initiator Message Checks	✓	✓	✓	✓	✓	✓
TDB.2.1.4.4.3.2	PROT-MSG-DATA-VDM-MODE-ACK	Discover Modes ACK Message Checks	✓	✓	✓	✓	✓	✓
TDB.2.1.4.4.4	PROT-MSG-DATA-VDM-ENTER-MODE	Enter Mode Message Checks	✓	✓	✓	✓	✓	✓
TDB.2.1.4.4.5	PROT-MSG-DATA-VDM-EXIT-MODE	Exit Mode Message Checks	✓	✓	✓	✓	✓	✓
TDB.2.1.4.4.6	PROT-MSG-DATA-VDM-ATT	Attention Message Checks	✓	✓	✓	✓	✓	✓
TDB.2.2.9.2	PROT-PROC-GETSRCAPS-UUT	Procedure and Checks for UUT Originated Get_Source_Cap			✓	✓	✓	✓
TDB.2.2.10.1	PROT-PROC-GETSNKCAPS-TSTR	Procedure and Checks for Tester Originated Get_Sink_Cap			✓	✓	✓	✓
TDB.2.2.10.2	PROT-PROC-GETSNKCAPS-UUT	Procedure and Checks for UUT Originated Get_Sink_Cap			✓	✓	✓	✓
TDB.2.2.11.1	PROT-PROC-GOTOMIN-TSTR	Procedure and Checks for Tester Originated GotoMin			✓	✓	✓	✓
TDB.2.2.11.2	PROT-PROC-GOTOMIN-UUT	Procedure and Checks for UUT Originated GotoMin			✓	✓	✓	✓
TDB.2.2.12.1	PROT-PROC-SR-TSTR	Procedure and Checks for Tester Originated Soft Reset			✓	✓	✓	✓
TDB.2.2.12.2	PROT-PROC-SR-UUT	Procedure and Checks for UUT Originated Soft Reset			✓	✓	✓	✓
TDB.2.2.13.1	PROT-PROC-HR-TSTR	Procedure and Checks for Tester Originated Hard Reset			✓	✓	✓	✓
TDB.2.2.13.2	PROT-PROC-HR-UUT	Procedure and Checks for UUT Originated Hard Reset			✓	✓	✓	✓
TDB.2.2.14	PROT-PROC-BIST-TSTR	Procedure and Checks for Tester Originated BIST			✓	✓	✓	✓

Source: USB-PD Test Plan Rev 1.0

# USB-PD Device Compliance Tests

## Secondary Checks



Test Ref #	Test Name	Test Description	Required Tests by Device Type				
			DRP	Provider	Consumer	Dual Role Device	
						C/P	P/C
		<b>Secondary Tests for all Devices</b>					
		<b>Secondary Message Checks</b> Performed whenever the Appropriat Message is Detected					
TDB.1.1.1	PHY-MSG-GEN	PHY Level General Message Test (SOP*)					
TDB.2.1.2.1	PROT-MSG-HDR	Message Header Checks - Except GoodCRC	✓	✓	✓	✓	✓

Test Ref #	Test Name	Test Description	Required Tests by Device Type				
			DRP	Provider	Consumer	Dual Role Device	
						C/P	P/C
		<b>Secondary Procedure Checks</b> Performed whenever the Appropriat Message is Detected					
TDB.2.1.2.2	PROT-MSG-HDR-C						
TDB.2.1.3	PROT-MSG-CTRL						
TDB.2.1.3.1	PROT-MSG-CTRL	TDB.2.2.1.1 PROT-PROC-AMS_1			✓	✓	✓
TDB.2.1.4.1.1	PROT-MSG-DATA	TDB.2.2.2.1 PROT-PROC-GOODCRC-TSTR			✓	✓	✓
TDB.2.1.4.1.2	PROT-MSG-DATA	TDB.2.2.2.2 PROT-PROC-GOODCRC-UUT			✓	✓	✓
TDB.2.1.4.2	PROT-MSG-DATA	TDB.2.2.3.1.1 PROT-PROC-SWAP-TSTR-SNK			✓		✓
TDB.2.1.4.3	PROT-MSG-DATA	TDB.2.2.3.1.2 PROT-PROC-SWAP-TSTR-SRC			✓		✓
TDB.2.1.4.4.1.1	PROT-MSG-DATA	TDB.2.2.3.2.1 PROT-PROC-SWAP-UUT-SNK			✓		✓
TDB.2.1.4.4.1.2	PROT-MSG-DATA	TDB.2.2.3.2.2 PROT-PROC-SWAP-UUT-SRC			✓		✓
TDB.2.1.4.4.2.1	PROT-MSG-DATA	TDB.2.2.4 PROT-PROC-PSSOURCEOFFTIMER			✓		✓
TDB.2.1.4.4.2.2	PROT-MSG-DATA	TDB.2.2.5 PROT-PROC-PSSOURCEONTIMER			✓		✓
TDB.2.1.4.4.3.1	PROT-MSG-DATA	TDB.2.2.6 PROT-PROC-PING			✓	✓	✓
TDB.2.1.4.4.3.2	PROT-MSG-DATA	TDB.2.2.7.1 PROT-PROC-REQ-TSTR			✓	✓	✓
TDB.2.1.4.4.4	PROT-MSG-DATA	TDB.2.2.7.2 PROT-PROC-REQ-UUT			✓		✓
TDB.2.1.4.4.5	PROT-MSG-DATA	TDB.2.2.8.1 PROT-PROC-SRCCAPS-TSTR			✓		✓
TDB.2.1.4.4.6	PROT-MSG-DATA	TDB.2.2.8.2 PROT-PROC-SRCCAPS-UUT			✓	✓	✓
		TDB.2.2.9.1 PROT-PROC-GETSRCCAPS-TSTR			✓	✓	✓
		TDB.2.2.9.2 PROT-PROC-GETSRCCAPS-UUT			✓	✓	✓
		TDB.2.2.10.1 PROT-PROC-GETSNKCAPS-TSTR			✓	✓	✓
		TDB.2.2.10.2 PROT-PROC-GETSNKCAPS-UUT			✓	✓	✓
		TDB.2.2.11.1 PROT-PROC-GOTOMIN-TSTR			✓		✓
		TDB.2.2.11.2 PROT-PROC-GOTOMIN-UUT			✓	✓	✓
		TDB.2.2.12.1 PROT-PROC-SR-TSTR			✓	✓	✓
		TDB.2.2.12.2 PROT-PROC-SR-UUT			✓	✓	✓
		TDB.2.2.13.1 PROT-PROC-HR-TSTR			✓	✓	✓
		TDB.2.2.13.2 PROT-PROC-HR-UUT			✓	✓	✓
		TDB.2.2.14 PROT-PROC-BIST-TSTR			✓	✓	✓

Source: USB-PD Test Plan Rev 1.0

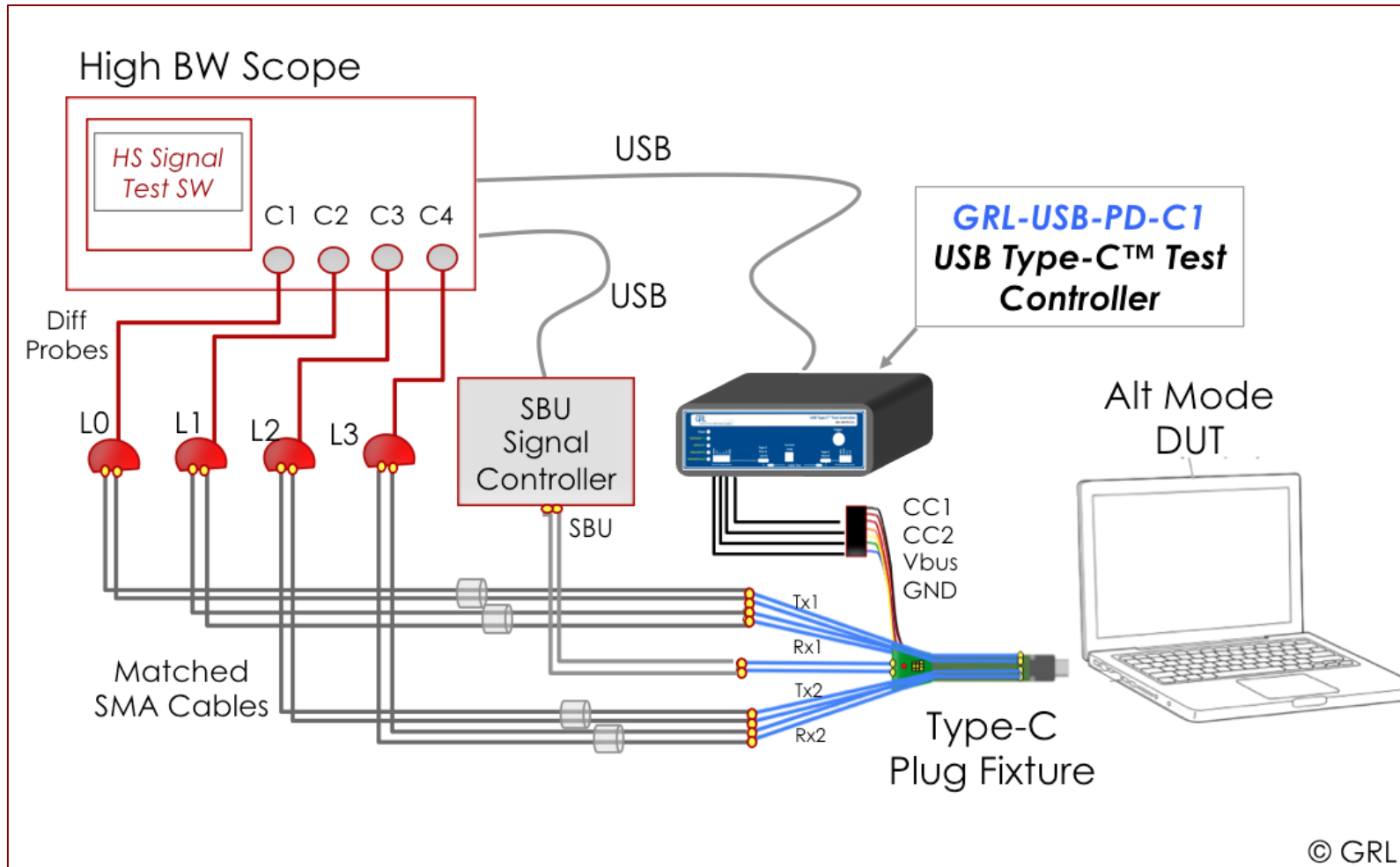


# DisplayPort over Type-C Testing

- **VESA Specifications addressed by GRL-USB-PD/C1 MOI-QS Guide**
  - *DisplayPort Alt Mode on USB Type-C Specification Standard Ver1.0a*
  - *DisplayPort Over Type-C CTS Draft (Jim Choate is Owner)*
- **DisplayPort Specific USB-PD Protocol Test Requirements**
  - Validation of DisplayPort VDM Header, Mode Entry/Exit, Mode Status, Configuration, and Attention.
- **PHY CTS Test Requirements**
  - PHY Source/Sink Shall be tested in 4 lane mode.
  - PHY Source/Sink Shall be tested in 2 lane mode SS USB Tx/Rx Mode xTalk (AKA '2+2') turned on.
  - PHY Source/Sink Shall be tested with Max Power and '2+2 xTalk' if DUT is a Power Provider

# DP Over Type-C PHY Testing

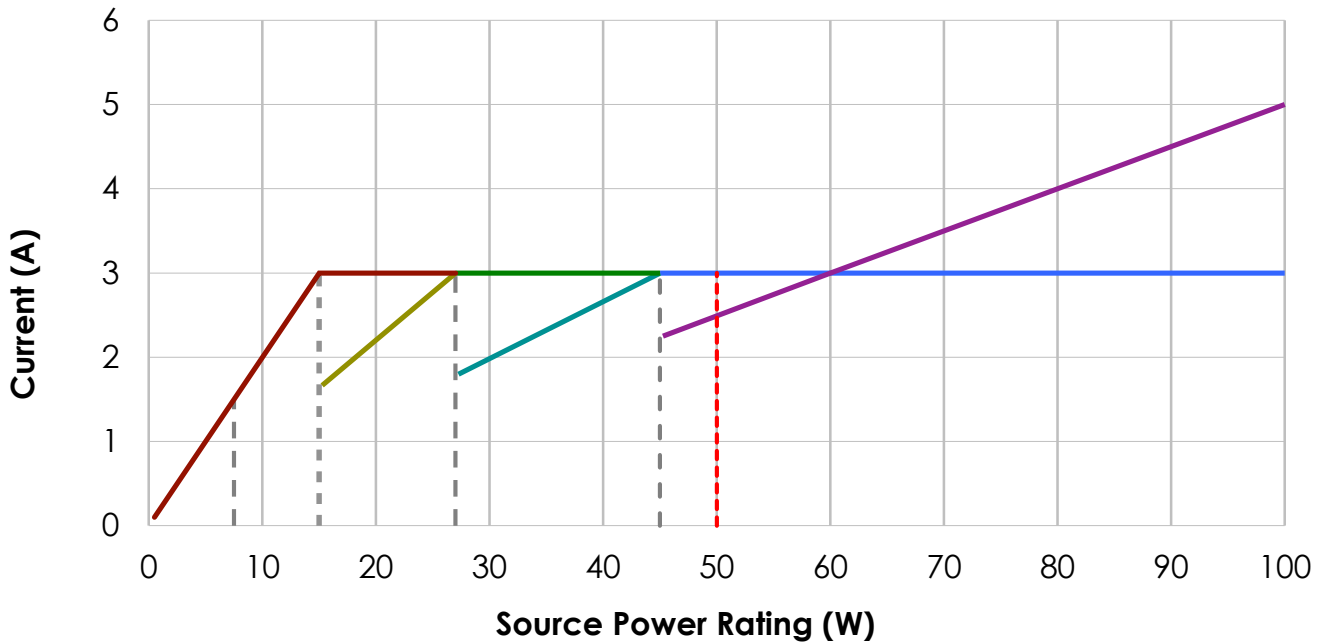
## 4 Lane Test Example



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PDP (W)	Current at 5V (A)	Current at 9V (A)	Current at 15V (A)	Current at 20V (A)
$0.5 \leq x \leq 15$	$x \div 5$			
$15 < x \leq 27$	3	$x \div 9$		
$27 < x \leq 45$	3	3	$x \div 15$	
$45 < x \leq 60$	3	3	3	$x \div 20$
$60 < x \leq 100$	3	3	3	$x \div 20^1$

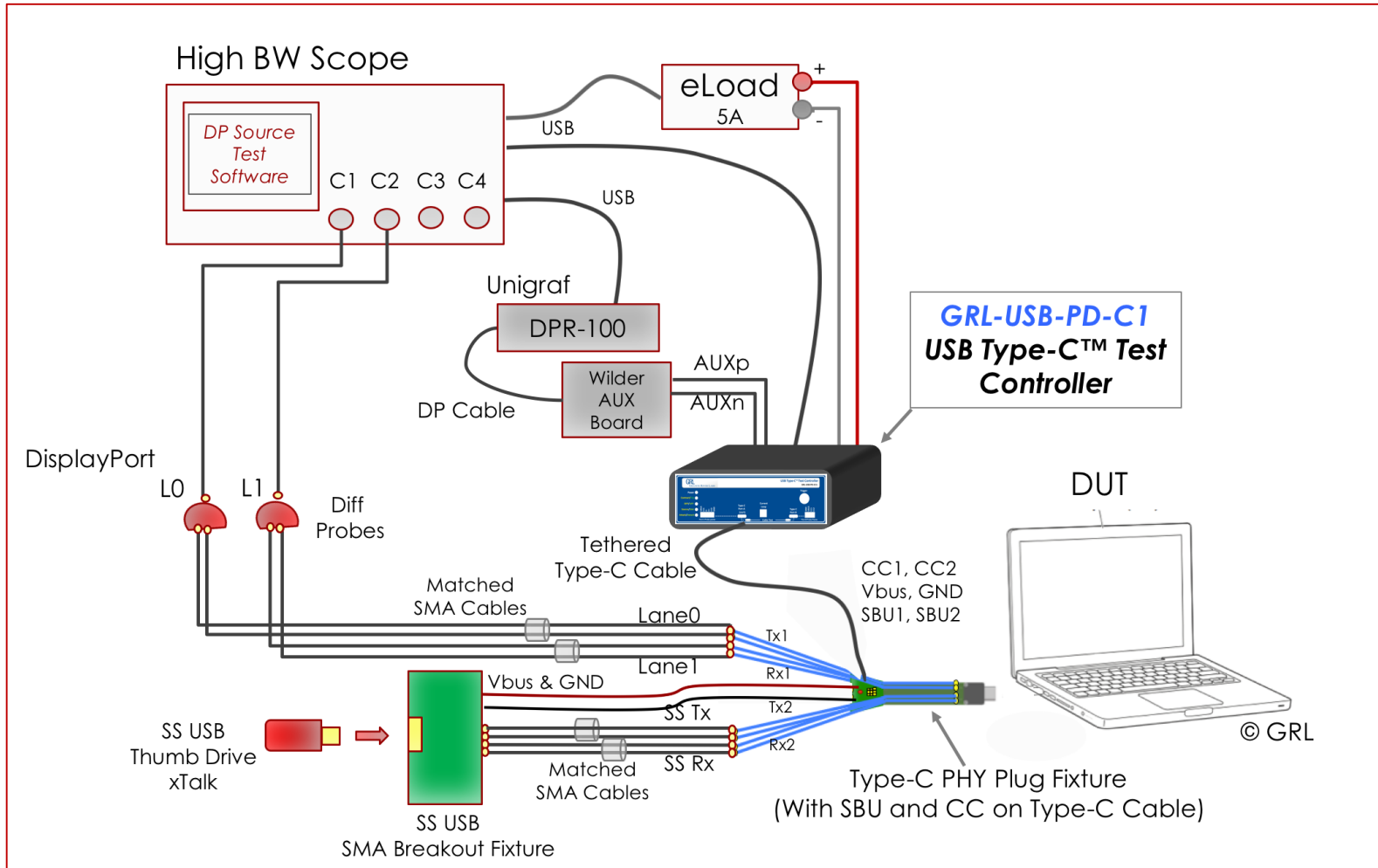
<sup>1</sup> Requires a 5A cable.



an example of an adapter with a rating at 50W. The adapter is required to support 20V at 2.5A, 15V at 3A, 9V at 3A and 5V at 3A.



# DP Over Type-C Source PHY Testing 2+2 with xTalk and Max Power



**\* Note: DP HPD/IRQ timing must be managed by the Controller PC (Scope) SW**



# Conclusions

- GRL has decades of experience in testing Electrical Interface Standards
- GRL has convenient locations in all Geographies
- GRL provides DP Over Type-C Logo Test Services
- GRL provides USB Power Delivery Compliance Test Solution (GRL-USB-PD) SW with SW (GRL-USB-PD-C1) Test Controller
- GRL's USB Type-C Test Controller can also be used as an 'Alt Mode Initiator' for DisplayPort PHY Testing
- GRL USB Type-C Test Services and Solutions are Available Today