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VESA DISPLAY STREAM COMPRESSION TASK GROUP

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Call for Technology: Advanced Display Stream Compression

TITLE: Call for Technology: Advanced Display Stream Compression

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Call for Technology: Advanced Display Stream Compression

1 Introduction

This document is a Call for Technology (CfT) to standardize a coding system for Advanced Display Stream Compression (A-DSC). The document includes requirements that apply to solutions, evaluation criteria, and required items to be submitted. VESA's goal is to standardize a visually lossless coding system to be used for compression of high-bandwidth video at lower compressed bit rates than are possible with DSC 1.1.

Proposals may be either full solutions, or may consist simply of possible tools or improvements that might be used to achieve the stated requirements.

2 Purpose and Requirements

2.1 Purpose

The advanced display stream coding system intends to meet these objectives:

- Target applications that require a lower bits per pixel (bpp) compressed bit rate than DSC 1.1 (i.e., significantly less than 8bpp) while still providing visually lossless subjective coding quality at least as good as DSC 1.1. In exchange for improved compression, A-DSC will require more complex encoders and decoders than DSC 1.1. As such, A-DSC is not intended to deprecate DSC 1.1; rather, it will complement it by allowing applications to target a different tradeoff of bpp versus complexity.
- Support TV and monitor panel resolutions larger than could be supported by DSC 1.1 in some systems with link bandwidth constraints
- Support mobile display resolutions larger than could be supported by DSC 1.1 in some systems with link bandwidth constraints
- Reduce the memory size required for frame buffer in display controller or driver IC applications

The advanced display stream coding system will have the following properties:

- On-the-fly, real-time coding with low complexity hardware and small-sized memory in both the encoder and the decoder. Higher complexity is allowable in an encoder than a decoder, since encoders tend to be implemented in more advanced technology than decoders, and generally encoders are more complex than decoders.
- Coded bit streams that can be transported over different link types

2.2 General Requirements

Proposals of a coding system shall include the attributes listed in the Table 1 and coding conditions listed in Table 2.

Table 1: Image Attributes for Proposals

Attribute	Values	Comments
Resolutions	Up to 10240 x 4320	Interlaced support is not specifically mandated.
Frame rate	Up to 120Hz	
Component type	RGB, YCbCr; full-range, i.e. each component ranges from 0 to 2^{bpc} -1 in integer format	Input type to the encoder shall match the output type of the decoder. Internal color space conversion is permitted, but if used, it shall be specified as part of the proposal and included in the model. See "component bit depth" for bpc definition
Component number	= 3	
Component bit depth	8, 10, 12, 14, or 16 bits	Referred to as bits per component (bpc) in this document
Sampling	4:4:4, 4:2:2 , 4:2:0	Sampling format at the input to the encoder and output of the decoder match. 4:2:2 and 4:2:0 modes should be designed to code more efficiently than using interpolated samples as is specified in Annex B of DSC 1.1.

Table 2: Coding Requirements for Proposals

Coding requirement	Values	Comments
Coding across frames	No, intra-frame only	The decoder shall be able to decode each slice using only data transmitted for that slice.
Required coded bit rate that ensures visually lossless coding of source content with no chroma sub-sampling (4:4:4)	8 bpc source: 4.8 – 6 bpp 10 bpc source: 6 bpp 12 bpc source: 6 – 9 bpp 14-16 bpc source: 9 bpp	The encoding process shall guarantee that the specified bpp rate is met for all content. This requirement applies for all values of image attributes. For cases where a range of bpp values are given, the lower bpp target may involve some compromises (e.g., additional cost/memory, higher viewing distance for visually lossless quality, etc.) Visually lossless quality shall be maintained through at least two generations (coding/decoding cycles).

Required coded bit rate that ensures visually lossless coding of source content with chroma subsampling (4:2:2 or 4:2:0)	4:2:2: 10% lower than 4:4:4* 4:2:0: 20% lower than 4:4:4*	Bit rate reduction is measured relative to the bit rate required for visually lossless coding of 4:4:4. * Refer to the bit rate targets specified in the previous row of this table.
Configurability	At minimum, attributes in Table 1; bpp and slice dimensions shall be configurable at least statically	Attributes may be modified at frame boundaries. Maximum bpp value shall be equal to half of the uncompressed bits/pixel value (for example, for 8bpc the maximum bit rate is 12bpp).
Throughput	See section 2.4.3	

Specific picture quality and other requirements are listed in Sections 2.3 and 2.4.

2.3 Picture Quality Requirements

The compression shall be visually lossless at the target bit rates for each given format in Table 2. Visually lossless means that the difference between the original image or image sequence and the same image or image sequence after compression and decompression is not detectable to the eye. Annex A specifies test methodologies Task Group members will use to evaluate proposals.

2.4 Other Requirements

2.4.1 Design Complexity

- Solutions should exhibit low complexity in terms of gate count, memory sizes, power, and clock rate requirement, and, once the quality metrics are met, the Task Group prefers low-complexity solutions over high-complexity solutions.

- Proposals shall describe the complexity from an encoder perspective, a decoder perspective, and a system-level perspective as it relates to the compression layer. The complexity of A-DSC is expected to be larger than DSC v1.1 in exchange for bit rate (bpp) improvement that also attains visually lossless quality.

- Proposals shall provide sufficient information to enable others to evaluate complexity.

- Samples are received by the encoder in a raster-scan order, and samples are likewise sent out from the decoder in a raster-scan order. If a solution requires block processing or other ordering, the complexity of the pixel reordering shall be included for both encoder and decoder size estimates. Block-based scanning may also be considered for some possible usage modes.

2.4.2 Encoder Behavior

DSC v1.1 defines an image will code into a single unique bitstream. The following paragraph allows an alternative solution.

Proposals wherein the encoder retains some information from one frame to the next to improve encoding will be considered. However, the complexity (and in particular the memory requirements) of such proposals need to be considered carefully. In any case correct decoding of bitstreams created by such encoders shall not depend on any retained information from any prior frame.

2.4.3 Pixel Processing Throughput

Each proposal shall show how the encoder and decoder operate for high throughput display streams, for instance, 8192 x 4320 at 120 Hz. If a proposed coding system uses design parallelism to meet real-time requirements, the proposals shall describe throughput and the method for parallel coding and decoding in the complexity analysis. Proponents shall specify the encoder and decoder throughput in terms of pixels per clock.

Encoder throughput shall be at least 1 pixel per clock, and 2 or 4 pixels per clock throughput is preferred. Decoder throughput shall be at least 2 pixels per clock, but 4 pixels per clock throughput is preferred. The complexity of a given solution will be considered in tandem with throughput; i.e., the total solution complexity is equal to the number of instances required times the per-instance cost plus any additional costs associated with having more than one instance.

2.4.4 Buffer Model

- The coding system shall guarantee, at minimum, real time operation with no overflow and no underflow of compressed data buffers at the encoder and decoder for any practical implementation in all configurations with all possible content. Proposals shall describe in detail how correct real-time behavior of encoder and decoder buffers is assured by the proposed algorithm and the sizes of those buffers.

- The encoder shall output streams at a Constant Bit Rate (CBR)[1]. CBR is defined as a constant number of bits per unit time, where a pixel is used as the unit of time. The bit rate shall be configurable at minimum statically (i.e., a fixed bit rate known to the encoder and decoder). The Task Group recommends that the coded bit rate can be programmable. If the rate is programmable, proponents should specify the range and resolution of the programming.

- Proponents should assume that the pixel input to the encoder and pixel output of the decoder represent the passage of time. The “bits per pixel” represents the number of compressed bits that are sent by the encoder and received by the decoder for each pixel time. See Figure 1 for an illustration of bit rate and CBR via an HRD (Hypothetical Reference Decoder) model.

- The Task Group recommends the inclusion of an HRD model, if applicable, to ensure correct real-time buffer operation. Refer to [Kerofsky and MacInnis, 2012].

[1] The Task Group acknowledges that DSC 1.1 supports variable bit rate (VBR) coding, but this requirement has been removed because the anticipated power savings of using VBR at A-DSC bit rates are not expected to justify the extra complexity.

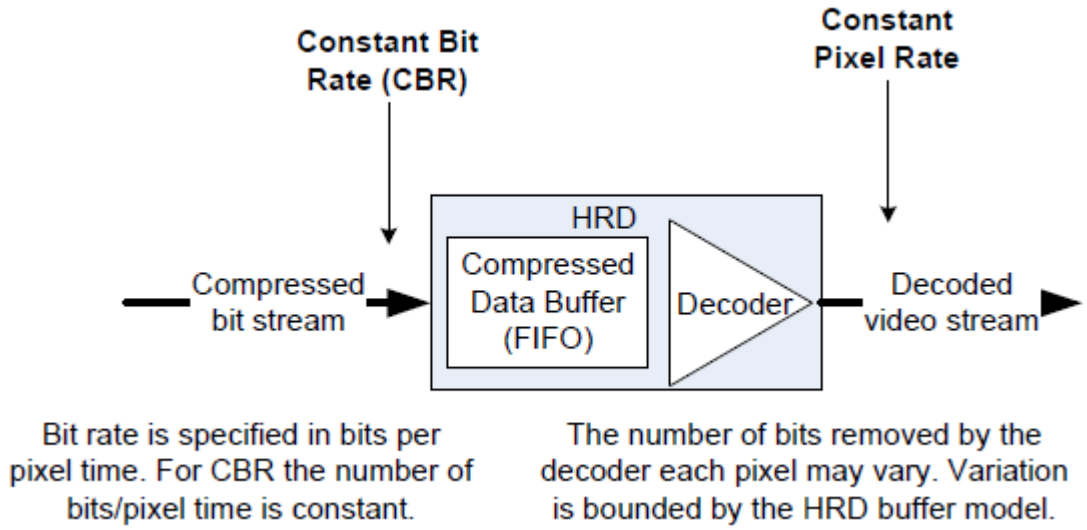

Figure 1: Illustration of Bit Rate via HRD

2.4.5 Transport

The means to transport the bitstream is outside the scope of this CfT. Coded streams may be transported via a variety of display links and transport schemes. The Task Group will favor proposals that require minimum changes and constraints to existing transport schemes, particularly those that have already adopted DSC 1.1. The future coding standard shall utilize a 128-byte PPS as defined in DSC 1.1, and the ***dsc_version_major*** and ***dsc_version_minor*** fields shall be located in the same bit fields as DSC 1.1 within the PPS. In addition, any slice multiplexing scheme shall create byte-aligned chunks of data in a manner similar to DSC 1.1.

2.4.6 Slice Support

This section discusses slices in order to support partial refresh, i.e. the ability of a source to send only a portion of a frame and update the corresponding portion of the image in a compressed frame buffer associated with a display. The following definition applies:

> **Slice:** A set of compressed bits that represents a specified set of samples. The set of samples forms a rectangle in the horizontal and vertical dimensions. This set of bits is independently decodable. Decoding of any one slice shall not depend on the availability of another slice nor on the decoded result of another slice.

Proposals are free to construct a slice from a plurality of smaller independently decodable blocks.

In order to support partial refresh schemes, the compression algorithm shall allow for update of part of an image using addressable slices. The number of bits allocated for each slice is constant for all content, and shall be equal to the target bits per pixel times the pixels per slice (perhaps rounded up by a small amount due to the byte alignment requirement imposed by the slice multiplexing). If a proposed coding system restricts slices by size or usage, the limitations should be documented. Allowing different slice widths within the same picture may be desirable for some applications, and proposals may describe methods by which this could be achieved.

In cases of panels containing a frame buffer, coded image or video data may be stored directly in the frame buffer without passing through a decoder. In this case, a partial frame update with independently coded slices may update a portion of the compressed frame in the frame buffer.

The number of slices per line is expected to be dictated primarily by considerations of throughput and the efficiency of partial frame updates. Different numbers of slices per line will be evaluated based on anticipated encoder and decoder clock speeds. The recommended slice height would be one that provides a good tradeoff of compression efficiency versus partial update size. For reference, the DSC 1.1 specification recommends a pixel count of >16,000 in each slice.

2.4.7 Error Recovery

The decoder is not expected to be resilient to bit errors. However, if a bit error occurs during a slice, the next slice received without error shall be processed correctly by the decoder. This implies that no state may be carried from one slice to another slice within a decoder.

3 Test Material, Coding Conditions and Anchors

3.1 Test Material

The test images and videos are available on the VESA shared work website (http://vesa.sharedwork.com) under Display Stream Compression/DSC Image Sets. Proposals will be tested against images on the website and other images that evaluators deem appropriate. The encoder under test has no prior access to any information about the content of each test image, such as content type.

3.2 Coding Conditions and Anchors

Image color space, bpc, chroma sampling, and resolution may vary with each test image.

4 Submission Requirements

Information on file formats and source code can be found in Annex B.

Proposals may include entire solutions or individual tools. Proposals shall include an overview presentation, source code (optional), and technical documentation. The technical documentation is not required to be a part of the initial submission; however, it will be required for each proposal before the Task Group decides to adopt the proposal. The inclusion of source code is optional but strongly recommended.

4.1 Overview Presentation

Each proposal shall include a presentation that provides a general overview of the proposal and associated complexity. This presentation may be either in Microsoft PowerPoint, Word document, or PDF format.

4.2 Source Code

Algorithm source code for tools or solutions shall meet the following requirements:

1) Configurable via command line or configuration file

2) Can be configured to different compressed bit rates (bpp) by the user (if applicable)

3) Can be configured to run either with the slice constraint from section 2.4.6 enforced or with a slice size of the proposer's choosing (if applicable)

4) Tools should provide a tangible benefit in complexity, performance, or both compared to some baseline (for example, DSC 1.1). Full solutions should meet all the stated requirements in this document.

Source code shall be documented and understandable. Assembly language is not permitted. All third-party libraries used by the source code shall be either public or provided in source code form with an appropriate license permitting unlimited and free re-use. Make files or project files shall support compilation on both Windows and Linux systems. The Task Group discourages submission of binary executables without source code.

4.3 Technical Documentation

Within two months of the initial submission, a technical description shall be submitted that includes:

- Theory of operation
- Coded bitstream syntax (if applicable)
- Coding process (encoding and decoding) methodology

The description shall include all necessary processing (including performance optimizations) that are used in the source code. The description shall show how the requirements in Section 2 of this CfT are met. Proponents are encouraged to list other features, benefits and performance advantages of their architecture or other assumptions explicit or implicit in the proposed architecture. Early submission of technical documentation, even if it is preliminary, is strongly encouraged.

The technical description shall contain sufficient information for experts to determine an approximate area and power for decoder and encoder implementations. The sizes of any on-chip or off-chip memories required for a hardware implementation shall be specified.

The technical description shall specify how the mandated throughput is achieved, including the relationship of clocks to pixels for all content. If achieving the mandated throughput requires additional complexity, that complexity shall be documented.

4.4 Submission of Technology Requirements

Proposers shall submit a completed and signed "Exhibit A: Submission of Technology Form" from VESA Policy 200C ("Intellectual Property Rights (IPR) Policy"), Section 12, at the same due date as proposals are due (see section 5 for schedule). VESA Policy 200C is available for download from the VESA website (http://www.vesa.org/join-vesamemberships/).

5 Timeline

The due dates for responses to this CfT and the A-DSC development schedule are provided below. Dates are subject to change at the discretion of the Task Group.

CfT Issued: January 15, 2015

Proposals due: April 15, 2015 (tentative face-to-face meeting in California to review technology submissions on April 20-22, 2015).

Test model available: June 1, 2015

Test model evaluation reports: October 1, 2015

Final tool selection: January, 2016

Draft specification: July, 2016

Adoption: September, 2016

6 Contacts and Submission Process

Please submit questions concerning this Call for Technology to the VESA Moderator at the below email.

Proponents shall contact the VESA Moderator to obtain customized instructions for uploading materials to an HTTPS-secured site on the VESA Work Zone. After acceptance by the Moderator, the uploaded proposals will be posted to the Work Zone and will be made accessible to VESA members. The Task Group will determine a suitable time to make all proposals simultaneously available for review.

Proponents shall be responsible for annotation of any items that are confidential within the submitted materials. Such annotation shall be subject to the conditions of VESA Policy 221C, "Document Disclosure and Distribution Policy". Any materials marked as confidential to a particular company or legal entity other than VESA will be rejected. Copies of VESA Policy 221C are available from the VESA Moderator for non-members.

Moderator email: moderator@vesa.org

7 References

Kerofsky, Louie, and Sandy MacInnis. "DSC Hypothetical Reference Decoder (HRD) Buffer Model Introduction." VESA Work Zone (Display Stream Compression, Past Months, 2012, HRD buffer model intro 121026.pdf), 2012.

"VESA Display Stream Compression (DSC) Standard Version 1.1." http://www.vesa.org/. 2014.

ANNEX A – Test Methodology

This annex provides information on how proposals will be tested.

A.1 Methodology

Testing will include still images, image sequences, and motion clips. Still images will be evaluated to see if any differences are visible when alternating views between the compressed and uncompressed versions without an intervening black frame. Some of this testing will be done in accordance with ISO/IEC DIS 29170-2.

Motion clips will be evaluated to see if any differences or artifacts are visible when sequentially alternating between the uncompressed and compressed versions. Evaluators may choose to evaluate images or videos side-by-side on one or two monitors as well.

Scrolling images will also be tested. A complex image may be scrolled one or more pixels/frame horizontally, vertically, or diagonally. Testing will include forced-choice subjective experiments comparing original and coded scrolling sequences. Images may also be processed by shifting, coding, and removing the shift, so that scrolling performance can be measured using an in-place alternating view test between images coded with different pixel offsets.

Objective metrics such as PSNR will not be used to ascertain whether a certain image is visually lossless or not.

A method to verify multi-generation coding quality is to be defined by the Task Group during the proposal phase of this coding system development. A final definition should be available to members and contributors no later than June 1, 2015.

A.2 Viewing Conditions

Since displays may be used in a wide variety of viewing conditions, the Task Group seeks to minimize specific limitations on the viewing conditions for this test. However, some limitations are provided in this section. Evaluators will document the viewing conditions used for the tests, such as peak brightness, calibration of the display, details about the display (model, type, subpixel arrangement, etc.), ambient lighting conditions, etc.

Since the compression system is targeted toward display links, zooming tests will not be considered for determining whether an image is “visually lossless” or not, although zooming may be used to help study artifacts. However, evaluators may look at realistic scaling scenarios (such as overscan or upscaling in a TV).

For 6 bpp, proposals will be evaluated using test setups with as few as 30 pixels per degree. For bit rates that are lower than 6 bpp, proposals may be evaluated at both 30 and 60 pixels per degree to determine if a greater number of pixels per degree can make artifacts more difficult to detect subjectively for lower bpp rates. Note, for a given display size and resolution, greater pixels per degree corresponds to greater viewing distance, and for a given viewing distance and display size, greater display resolution corresponds to greater pixels per degree.

Motion clips will be run at frame rates that maximize the visual perception of artifacts (typically 6-15 Hz) for conservative testing, while recognizing that practical applications are expected to use frame update rates of at least 24fps and typically 60fps or 120fps. Interleaved image trials shall use equal numbers of frames for original and compressed images. For example, a 6 Hz interleaving rate on a 60 Hz display is achieved by alternating 5 frames of an original image and 5 frames of a reconstructed image. Likewise, scrolling rates will be chosen so that each reconstructed image is presented for an identical number of frame times.

A.3 Content Types

Many types of still images will be evaluated: continuous tone images, landscapes, people portraits, animals, fine text, web pages, graphics, computer screen captures with or without sub-pixel rendering, etc. Test patterns such as noise and zone plates will be evaluated, but some visual loss may be tolerated on certain patterns.

Video tests will include movies, television, computer games, graphics, etc. Source video may be compressed using a standard broadcast compression algorithm before compression testing (e.g., MPEG-2, AVC, HEVC, etc.).

A.4 High Dynamic Range (HDR) Testing

Testing will include high dynamic range displays and content. Content will include BT.2020 10 and 12 bpc source as well as content sourced from other optical-electrical transfer functions (OETF). To cover different color gamut usage modes, content with sRGB, BT.709, and BT.2020 primaries will be tested.

Very bright displays (1000+ nits) will be used for some of the HDR testing.

ANNEX B – Model Image File Types and Filename Conventions

The submitted models shall support uncompressed DPX (SMPTE-268M) and PPM (RGB modes only) for both image input and output. DPX can support a variety of color spaces, bpc, and color subsampling. For output files, the following fields in the DPX are required to be valid:

In the image header: PixelsPerLine and LinesPerElement

In image element: Descriptor, BitSize, and Packing

The Task Group recommends proponents utilize the utility functions in the DSC 1.1 C model in order to expedite the integration of proposed tools into a test model.

Some other suggestions for source code:

- Provide C interfaces/wrappers for non-C code.
- Utilize the picture structures in vdo.h of the DSC 1.1 source code. The command-line and script file parser is also useful.
- Focus the code on the algorithm itself, not a possible implementation. Keep it as simple as possible.
- Document the code thoroughly.
- Support an encode mode, a decode mode, and an encode/decode mode.