



# VESA Display Stream Compression

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## OVERVIEW

Display manufacturers are turning to higher-resolution displays to differentiate their products. The increased pixel counts have required increased bandwidth over the links that drive these displays. However, advances in physical layer technology have not kept up with the increases in pixel counts. In addition, some display driver ICs store displayed frames, so higher-resolution displays mean larger on-chip frame buffers. These factors have created a need for compression on display links. The Video Electronics Standards Association (VESA®), in liaison with the MIPI® Alliance, has developed an industry standard (Display Stream Compression 1.0) for interoperable, visually lossless compression over display links.

This whitepaper discusses the challenges that high-resolution displays present, the ways that the DSC algorithm uniquely addresses these challenges, and the methods that were used to achieve the desired picture quality.

## BACKGROUND

Display links are everywhere, connecting computers to monitors, set-top boxes to televisions, and application processors to display panels. With the successful marketing of very high pixel density displays, consumer demand for higher

resolutions has skyrocketed, which means that the amount of pixel data sent over display links has skyrocketed as well. Some links are simply not capable of handling the extra bandwidth, and those that are have become expensive and power-hungry. Some display interfaces now support carrying multiple video streams, which also burdens the physical layer underlying these interfaces.

Many companies have tried to address these problems by introducing image compression on the pixel data. Unfortunately, these schemes are frequently not visually lossless, are poorly documented, or are difficult and expensive to implement in a conventional display device. Proprietary solutions run significant risks of not being interoperable. Source and display implementers typically pay a high development cost to implement a single compression scheme. Source implementers want their products to work with any display device, and implementing all possible proprietary compression schemes is simply impractical. And display implementers require compression that provides interoperability and excellent picture quality at a low cost.

In late 2012, VESA recognized the need for an industry-standard display stream compression specification and formed the Display Stream Compression (DSC) task group. The goal was to create a compression standard that display link standards could directly refer to, enabling source and display manufacturers to implement a single, well-documented compression specification across all products and interfaces.

The group issued a call for proposals in January, 2013, evaluated six different proposals, and selected the one that best met the requirements:

- The picture quality must be good enough that users cannot tell that the compression is active (i.e., visually lossless).
- The compressed data rate should be constant, and the algorithm must be visually lossless at rates as low as 8 bits/pixel.
- Some applications require the ability to update small regions of the image, so the specification needs to support independently decodable regions (i.e., slices).
- Many different video formats must be supported (RGB, YCbCr 4:2:2, or 4:4:4; 8, 10, or 12 bits/component).
- The scheme must be easy and inexpensive to implement in real-time using conventional hardware, and it should be possible to implement decoders using older technologies and process nodes.

Existing video compression standards do not meet these requirements. Transform-based algorithms, such as MPEG-2 and H.264, and wavelet-based algorithms, such as JPEG-2000 and VC-2, require the storage of many lines of pixel data, which is too expensive. JPEG-LS cannot guarantee a constant bit rate and does not meet the quality requirement when configured for lossy coding. So there is no existing specification that meets these requirements.

## ALGORITHM OVERVIEW

The DSC encoding algorithm is based on delta pulse code modulation (DPCM) with an Indexed Color History (ICH). It requires a single line of pixel storage and a rate buffer. An encoder block diagram is shown in Figure 1.

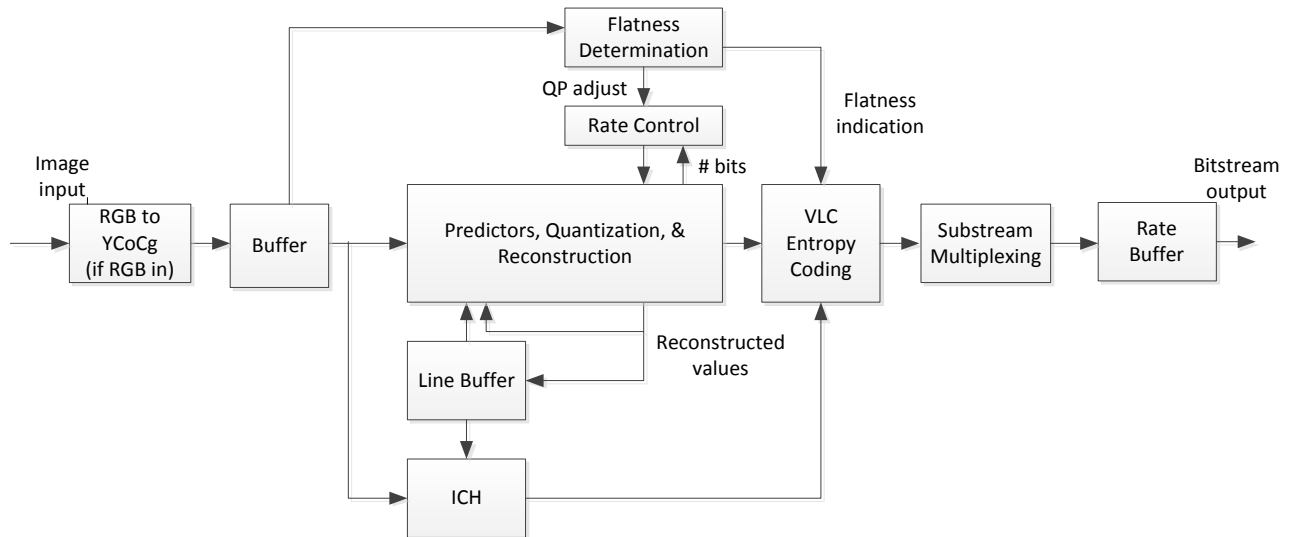


Figure 1 – DSC encoder block diagram

The main pieces of an encoder are:

- **Color-space conversion.** RGB inputs are converted to YCoCg-R<sup>1</sup> for encoding. This process is simple and involves only shifts and additions.
- **Prediction.** Three modes are supported:
  1. A modified version of median-adaptive prediction<sup>2</sup>. The median-adaptive predictor is used in JPEG-LS. The modification allows parallel prediction of three consecutive sample values.
  2. Block prediction. This predicts samples from previously reconstructed pixels to the left. Both encoders and decoders perform an identical search on reconstructed pixels to determine the block prediction usage, so no bits are sent. Due to the hardware cost of the search, block prediction is optional for decoders.
  3. Midpoint prediction. This predicts samples using the midpoint of the component range. This mode bounds the number of bits required to code even worst-case samples.
- **Quantization.** A power-of-2 quantizer can be easily implemented using a shifter.

<sup>1</sup> Malvar, H., G. Sullivan, and S. Srinivasan. "Lifting-based reversible color transformations for image compression." Proc. SPIE, Vol. 7073. 2008.

<sup>2</sup> Martucci, S. "Reversible compression of HDTV images using median adaptive prediction and arithmetic coding." IEEE Int. Symp. Circuits & Systems, Vol 2. 1990.

- **Reconstruction.** This involves adding the inverse quantized residual to the predicted value and ensuring the result does not fall outside the valid range of sample values.
- **Indexed Color History (ICH).** Recently used pixel values are stored and can be referenced directly using a special syntax.
- **Rate control.** The quantization parameter is adjusted based on the buffer fullness and image activity to maximize picture quality while ensuring that the rate buffer does not overflow or underflow when operating at the indicated bit rate.
- **Flatness detection.** Transitions from non-flat to flat areas are signaled in the bitstream to reduce quantization artifacts.
- **Entropy encoder.** Prediction residuals are coded using a novel form of entropy coding, which is easy to implement in hardware that can encode or decode three samples per clock per substream encoder or decoder.
- **Substream multiplexing.** A headerless packet multiplexing scheme is employed to allow three entropy decoders to run in parallel on the decoder side, which facilitates decoding 3 pixels per clock. Decoders can perform the demultiplexing easily, since the packet order is optimized for decoding efficiency.

## PERFORMANCE

From a picture quality standpoint, the DSC algorithm outperforms many proprietary algorithms. The algorithm was rigorously tested by experts on a variety of mobile and large-panel display types. All types of test content were included:

- White noise, zone plates, multiburst, and other test patterns
- High-density subpixel rendered text (for example, Microsoft ClearType™)
- Computer, phone, and tablet screen captures
- Photos and video

Several methods were used to confirm the visually lossless performance of the algorithm. Most commonly, the original image and uncompressed image were flipped back and forth in place on the same screen to determine if the user could see a difference. The images were selected for their difficulty. One company analyzed thousands of images gathered from the internet and selected those that were most likely to have artifacts based on a mathematical analysis of the compressed images. The selected images were subjected to the flipping test. All of the analyses showed that the DSC algorithm outperformed five other proprietary algorithms on these picture quality tests, and was either visually lossless or very nearly so for all tested images at 8 bits/pixel.

## CONCLUSION

The DSC standard provides designers of source and display devices a visually-lossless, standardized way to transfer more pixel data over display links and to save memory size in embedded frame buffers in display driver ICs (DDICs). DSC

is suitable as a compression method for many interface specifications, such as MIPI Display Serial Interface (MIPI DSI), DisplayPort™, embedded DisplayPort (eDP), and others. DSC provides the capability to allow 8Kp60 video over DisplayPort, 4Kp60 video over dual-link MIPI DSI, or WQXGA at 60 Hz over single-link MIPI DSI. Many leading consumer electronics and integrated circuit manufacturers were involved in the ratification of this standard.

The specification includes a C model that can be used for design verification and testing. Compliance tests, test images, and an application note are currently under development and will be released shortly.

The standard is available for free to VESA members and for \$350 for non-members. For more information on DSC, please visit <http://www.vesa.org/>.

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