DisplayPort Derivatives: eDP and MyDP and Considerations of Physical Layer Test

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Topics

DisplayPort Technology

eDP and MyDP

Capabilities

Testing Considerations
Something Good is Happening...

Standard DisplayPort

Computing

eDP

Embedded Systems

Consumer Electronics

MyDP

Portables

VESPA: 200 members strong!
DisplayPort Technology Rollouts

- **Standard DP**
  - DP1.0
  - DP1.1

- **eDP 1.0**
  - IDP 1.0
  - DP1.2
    - 5/2012
    - 12/2012

- **MyDP**
  - Specification Released
  - CTS Released
  - 1.0
    - 5/2012
  - 1.2
    - 1/2013
  - 1.3
    - 7/2013

- **Today**
  - 5/2013

- **5/2012**
- **4/2013**
- **7/2013**
<table>
<thead>
<tr>
<th>Standard DisplayPort</th>
<th>Capabilities</th>
<th>Competing Technology</th>
<th>Noteworthy Features</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1,2, or 4 lanes</td>
<td>HDMI DVI? VGA?</td>
<td>Integrable in low geometry silicon. Dominating in PCs now.</td>
</tr>
<tr>
<td></td>
<td>Four Settings for Lvl and Pre-emph SSC 3 bit rates</td>
<td></td>
<td></td>
</tr>
<tr>
<td>eDP</td>
<td>1,2, or 4 lanes</td>
<td>LVDS MIPI</td>
<td>Low Power rivals MIPI. High data rates supported now. Attributes similar to DP</td>
</tr>
<tr>
<td></td>
<td>Multi-Level Pre-emph SSC Multi bit rates</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MyDP</td>
<td>1 lane</td>
<td>MHL</td>
<td>1080p/60 24 bit color achieved. Many connection models. Attributes same as DP</td>
</tr>
<tr>
<td></td>
<td>Four Levels Pre-emphasis SSC 3 bit rates</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Why Successful?

- 200 member companies participating
- Original DP foundational principles serving DP extensions
- Consumer focus in handling Legacy designs
- Interoperability Program/Self testing/Compliance testing
- Knowledgeable and Aggressive leaders

Craig Wiley
Parade Technologies

Alan Kobayashi
ST Micro
Key Features of DisplayPort

- **AUX Channel**
  - Very robust channel
  - Setup Link/Maintain Link
  - Test Assistance

- **uPacket Based**
  - Not based on Raster timings
  - Fixed bit rates

- **Physical Layer Features**
  - Multiple Bit rates
  - Multiple Levels
  - Multiple Pre Emphasis Settings
  - Spread Spectrum Clocking
DisplayPort Link

The AUX Channel enables Link setup and maintenance as well as control for testing.
AUX Channel Implementation
Manchester II Signaling

Figure 3-22: AUX CH Differential Pair

Figure 3-23: Self-clocking with Manchester-II Coding

Figure 3-24: AUX CH SYNC Pattern and STOP Condition
MyDP: Portable → TV

Today: MyDP Connectivity

In the Future: Wireless from your portable
Your Entertainment System

My Entertainment System
Transmission Requirements

4k x 2k? No Way! Not Yet Anyway

Using HDMI transmission as a benchmark...

<table>
<thead>
<tr>
<th>Timing</th>
<th>1080i/720p</th>
<th>1080p/8bit</th>
<th>1080p/10bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lane Bit Rate</td>
<td>750Mbs</td>
<td>1.50Gbs</td>
<td>1.87Gbs</td>
</tr>
<tr>
<td>Pixel Rate</td>
<td>75MPs</td>
<td>150MPs</td>
<td>187MPs</td>
</tr>
<tr>
<td>Composite Bit Rate</td>
<td>2.23Gbs</td>
<td>4.46Gbs</td>
<td>5.57Gbs</td>
</tr>
</tbody>
</table>

Display Technologies Available:
- DisplayPort: Maximum Lane Rate--5.4Gbs
- HDMI: Maximum Lane Rate---------3.4Gbs
Let's Look Closer...

For both MHL and MyDP the uUSB connector is the de facto connector, but it is not find it mentioned in either standard!

MyDP does not specify either a connector type or a pin-out of a connector connecting a MyDP Source device to a MyDP-to-DP cable adaptor other than stating that it can be mapped to a connector with as few as five pins and that the electrical specification must be met at the MyDP connector pins as specified in Section 8.

D- and D+ is the differential data lane

ID: USB mode detect

Conclusion: There is only one data lane through which the composite data rate must be conveyed. So the composite bit rate rate is the metric.
Getting down to One data lane...

DisplayPort

20 Pins

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Signal Type</th>
<th>Pin Name</th>
<th>Mating Row</th>
<th>Vertex Opposite</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>In</td>
<td>ML_Lane 3(n)</td>
<td>Top</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>GND</td>
<td>Bottom</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>In</td>
<td>ML_Lane 3 (p)</td>
<td>Top</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>In</td>
<td>ML_Lane 2 (n)</td>
<td>Bottom</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>GND</td>
<td>Top</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>In</td>
<td>ML_Lane 2 (p)</td>
<td>Bottom</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>In</td>
<td>ML_Lane 1 (n)</td>
<td>Top</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>GND</td>
<td>Bottom</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>In</td>
<td>ML_Lane 1 (p)</td>
<td>Top</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>In</td>
<td>ML_Lane 0 (n)</td>
<td>Bottom</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>GND</td>
<td>GND</td>
<td>Top</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>In</td>
<td>ML_Lane 0 (p)</td>
<td>Bottom</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>CONFIG</td>
<td>CONFIG1</td>
<td>Top</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>CONFIG</td>
<td>CONFIG1</td>
<td>Top</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>IO</td>
<td>AUX CH (p)</td>
<td>Top</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>GND</td>
<td>GND</td>
<td>Bottom</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>IO</td>
<td>AUX CH (n)</td>
<td>Top</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Out</td>
<td>Hot Plug Detect</td>
<td>Bottom</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>RTN</td>
<td>3 Green</td>
<td>Top</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>Power Out</td>
<td>TRI-Pin</td>
<td>Bottom</td>
<td></td>
</tr>
</tbody>
</table>

- AUX+/-, HPD Config1/2
- 4 data lanes
- 1 low speed line
- Power, Ground

MyDP

5 Pins

Power, Ground

Micro USB Male connector
MyDP

Spec Released: 1.0
Compliance Testing starting: June 2013
Maximum Data Rate: 5.4Gbs to support 1080p/60Hz
One could say that MyDP is not very new! It is just one lane DisplayPort!

There are other changes to get to 5 pin interface, but nothing changes in the high speed signaling.

Subsequent slides will be paired; the first to show the standard DisplayPort attributes and the next those for MyDP.
DisplayPort Technology

- 1 to 4 unidirectional high speed lanes
  - Fixed data rate independent of display raster (refresh)
- Auxiliary channel for link communication and auxiliary data flow
  - Link Setup and Maintenance (1Mb/s - Manchester II)
  - USB 2.0 Transport (Fast AUX -540Mb/s - standard 8b/10b)
- Auto detect of cable plug/unplug
MyDP Technology

- 1 unidirectional high speed lane
  - Fixed data rate independent of display raster (refresh)
- Auxiliary channel for link communication and auxiliary data flow
  - Link Setup and Maintenance (1Mb/s - Manchester II)
  - Single Ended
- Polling detect of cable plug/unplug
DP Technology: Specifications

Silicon structures:

- Structure leveraged from PCI Express
- Implementable on sub 65nm process
- Termination Voltage must be <2volts (internal to IC)

Receiver

- PLL BW=10MHz effective. Jitter tolerance curve specified.

Data Rate

- 1.62 Gbs (RBR)
- 2.7 Gbs (HBR) [units supporting HBR must support RBR]
- 5.4Gbs (HBR2) [units supporting HBR2 must support HBR]
MyDP Technology: Specifications

Silicon structures:

- Structure leveraged from PCI Express
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- Termination Voltage must be <2volts (internal to IC)

Receiver

- PLL BW=10MHz effective.
  Jitter tolerance curve specified.

Data Rate

- 1.62 Gbs (RBR)
- 2.7 Gbs (HBR)
- 5.4Gbs (HBR2)
DP Technology: Main Link Lanes

Lanes

• Each lane is Differential, 100Ω.
• 1, 2, 4 lane models for video data transport. 4 lane model capable must support 1 & 2 lane models. 2 lane model must support 1 lane model. Lanes are uni-directional.
• ANSI standard 8b/10b.
• Each lane has separate clock recovery from its data. No Explicit Clock.
• Single ended lines of each lane are source and sink terminated and biased. No external pull-up is needed for test equipment.
MyDP Technology: Main Link Lane

Lanes

• Each lane is Differential, 100Ω.
• 1 lane for video data transport. Lane is uni-directional.
• ANSI standard 8b/10b.
• Clock recovery from the data.
• Single ended lines of each lane are source and sink terminated and biased. No external pull-up is needed for test equipment.
DP Technology: Signal Attributes

- Four swing settings:
  - Setting 0: 400mV nominal
  - Setting 1: 600 mV nominal
  - Setting 2: 800 mV nominal
  - Setting 3: 1200 mV nominal (optional)

- Four Pre-Emphasis settings
  - Setting 0: 0 dB nominal
  - Setting 1: 3.5 dB nominal
  - Setting 2: 6 dB nominal
  - Setting 3: 9.5 dB nominal (optional)

Compliance Test Specification emphasizes monotonicity not accuracy

- No combination of voltage and pre-emphasis can exceed 1200mVolts p-p

- Spread Spectrum Clocking
  - (30-33KHz spreading frequency, downspread)
DP Technology: AUX Channel, DPCD

- Designated Control Link lane called ‘the AUX Channel’ specified. Operates at 1Mbs and is used in Link Training and Link Management and is Bidirectional Half Duplex.
- The Transmitter is the master.
- Receiver gains attention by pulling down on the Hot Plug Detect line.
- Manchester II coding (shown subsequently)

![Diagram of DP Technology: AUX Channel, DPCD]
MyDP: AUX Channel, DPCD

- Designated Control Link lane called ‘the AUX Channel’ specified. Operates at 1Mbs and is used in Link Training and Link Management and is Bidirectional Half Duplex.
- The Transmitter is the master.
- Receiver identified by polling. Link serviced by occasional DPCD reads.
- Manchester II coding (shown next page)
DP AUX Channel Implementation
Manchester II Signaling

Figure 3-22: AUX CH Differential Pair

Figure 3-24: AUX CH SYNC Pattern and STOP Condition

Figure 3-23: Self-clocking with Manchester-II Coding
MyDP AUX Channel Implementation
Manchester II Signaling, Single Ended

Figure 3-24: AUX CH SYNC Pattern and STOP Condition

Figure 3-23: Self-clocking with Manchester-II Coding
MyDP connection requirements.

High-level view

Zoomed-in view
Testing MyDP

MyDP Transmitters
- ✓ AUX-HPD
- ✓ Power Charging
- ✓ Waveform Parametrics
- ✓ Video/Audio Protocol Validation

MyDP Receivers
- DisplayPort!
- ✓ Power Charging
- ✓ Video/Audio Protocol Response
- ✓ Receiver Sensitivity/Jitter Tolerance (using test mode BER counting)
Test Fixtures

These are the MyDP fixtures from Wilder Technologies.
MyDP Fixture Schematic

From Wilder:
MyDP Source Testing

The test suite for standard DP applies for MyDP.
Preparing for Test
Control of your MyDP Device

Agilent DisplayPort Test Application

Set up your device

Main Link Phy Tests
Single ended AUX Tests

Set up your device
MyDP source testing is at TP2 only

Eye Diagram

Jitter: Non ISI, Total Jitter, HBR2 RJ/DJ/TJ

Non Pre-Emph Level

Main Link Frequency

Pre-Emphasis Level

AUX Eye

Intra Pair Skew

AUX Sensitivity
MyDP Sink Testing

MyDP ‘Sink’ Calibration and Test

Test Equipment

Signal Conditioning

Calibration

uUSB Plug

Test

VGA
DVI
HDMI
DP

Dongle

The test suite for standard DP applies for MyDP. Specs are different
Sink Test Jitter Components (RJ+DJ +ISI)

N4903B JBERT

Sink Device

Loop Back

Rec

Rx

Chip

Error Detection

FER: 0.757E-4

ISI
Summary of MyDP

MyDP is merely 1 lane DP so no modifications on the main link or protocol. Only significant change is that the AUX lane is Single ended, and therefore, the AUX sensitivity is halved.

MyDP can do 1080p/60 with 24 bits of color.

Same Connector, uUSB as MHL. Nothing else in common!
Huge changes from eDP 1.3

<table>
<thead>
<tr>
<th>Attribute</th>
<th>eDP 1.3</th>
<th>eDP1.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Levels</td>
<td>4 (std DP)</td>
<td>6 (200mv-450mV) Arbitrary allowed</td>
</tr>
<tr>
<td>Bit Rates</td>
<td>3 (std DP)</td>
<td>7 (1.45 to 5.4Gbs) Arbitrary allowed</td>
</tr>
<tr>
<td>Pre-Emphasis</td>
<td>4 (std DP)</td>
<td>Arbitrary</td>
</tr>
<tr>
<td>Panel Self Refresh</td>
<td>Whole frame only</td>
<td>Partial Frame enabled</td>
</tr>
<tr>
<td>Compression</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Multi-touch</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>BackLight control</td>
<td>Yes</td>
<td>Yes Regional control as well</td>
</tr>
</tbody>
</table>
AUX Channel Extended
### Levels/PreEmphasis/BitRates

<table>
<thead>
<tr>
<th>Link Rate Name</th>
<th>Parameter (Per Lane)</th>
<th>Nominal Per-lane Transfer Rate (Gbps/Lane)</th>
<th>Nominal Unit Interval (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>R162 (RBR)</td>
<td>Transfer Rate 1</td>
<td>1.62</td>
<td>617</td>
</tr>
<tr>
<td>R216</td>
<td>Transfer Rate 2</td>
<td>2.16</td>
<td>463</td>
</tr>
<tr>
<td>R243</td>
<td>Transfer Rate 3</td>
<td>2.43</td>
<td>412</td>
</tr>
<tr>
<td>R270 (HBR)</td>
<td>Transfer Rate 4</td>
<td>2.7</td>
<td>370</td>
</tr>
<tr>
<td>R324</td>
<td>Transfer Rate 5</td>
<td>3.24</td>
<td>309</td>
</tr>
<tr>
<td>R432</td>
<td>Transfer Rate 6</td>
<td>4.32</td>
<td>231</td>
</tr>
<tr>
<td>R540 (HBR2)</td>
<td>Transfer Rate 7</td>
<td>5.4</td>
<td>185</td>
</tr>
</tbody>
</table>

#### Transition Vdiff<sub>P-P</sub>

<table>
<thead>
<tr>
<th>Non-transition Vdiff&lt;sub&gt;P-P&lt;/sub&gt;</th>
<th>Transition Vdiff&lt;sub&gt;P-P&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Training Pre-emphasis 0</td>
</tr>
<tr>
<td>200mV</td>
<td>200mV</td>
</tr>
<tr>
<td>250mV</td>
<td>250mV</td>
</tr>
<tr>
<td>300mV</td>
<td>300mV</td>
</tr>
<tr>
<td>350mV</td>
<td>350mV</td>
</tr>
</tbody>
</table>

#### Non-transition Vdiff<sub>P-P</sub>

<table>
<thead>
<tr>
<th>Non-transition Vdiff&lt;sub&gt;P-P&lt;/sub&gt;</th>
<th>Transition Vdiff&lt;sub&gt;P-P&lt;/sub&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Training Pre-emphasis 0</td>
</tr>
<tr>
<td>300mV</td>
<td>300mV</td>
</tr>
<tr>
<td>350mV</td>
<td>350mV</td>
</tr>
<tr>
<td>400mV</td>
<td>400mV</td>
</tr>
<tr>
<td>450mV</td>
<td>450mV</td>
</tr>
</tbody>
</table>
Reference Equalizers (for measurements only)
Test Points Available

- eDP Test Point
- Test Fixture & Test Model
- Test at a Modified TP2
Testing eDP

1. Lots of bit rates and levels and arbitrary settings are allowed.
2. TestPoint is TP3, the cable is considered part of the source.
3. A Test guideline is being created now. Mike Hamann of Intel is leading this effort.

**VESA® eDP1.4 PHY Compliance Test Guideline, Version 1.0**

**OPEN ISSUES:**
- HBR2 Pattern CP2520,
- Data Rate Measurement (SSC),
- TX AUX Channel Eye Derivation
- RX AUX Over-Sampling Assumptions
Testing eDP

eDP source testing is at TP3 only. Equalizers need to be applied to overcome losses of channel generally.

eDP sink evaluation is typical TP3 testing.

Eye after Channel (TP3)

Eye after Equalizer (TP3Eq)
AUX Channel Testing

AUX Eye Testing

**Source Initiation of AUX communication**

**Receiver Response to Source AUX**

AUX Sensitivity

Reduce the Rx device’s AUX level. (100mV shown, 240 spec’d)
eDP1.4 Fixturing
Testing eDP

A couple of points to make:

1. There is no official compliance program—its embedded so interoperability with other vendors is not a requirement.

2. Use your own connector or pinout → Create your own fixture!

3. Advise to consider validation/verification issues early in process. HPD, Test Mode, level groups.

4. What is tested will be driven by you and your vendor/customer.
DisplayPort Technology

Continue to expect VESA will continue rolling out value-added capabilities in Display Technologies. Our foundation is solid.

200 members strong—> Industry richness in participation to address the transport and rendering of Display information.

Testing and validation is a core component of our interoperability program and is seen as an ecosystem enabler.