DisplayPort Derivatives: eDP and MyDP and Considerations of Physical Layer Test

Brian Fetz

May 6th, 2013

Topics

DisplayPort Technology

eDP and MyDP

Capabilities

Testing Considerations

Something Good is Happening…

Standard DisplayPort

Computing

eDP

Embedded Systems

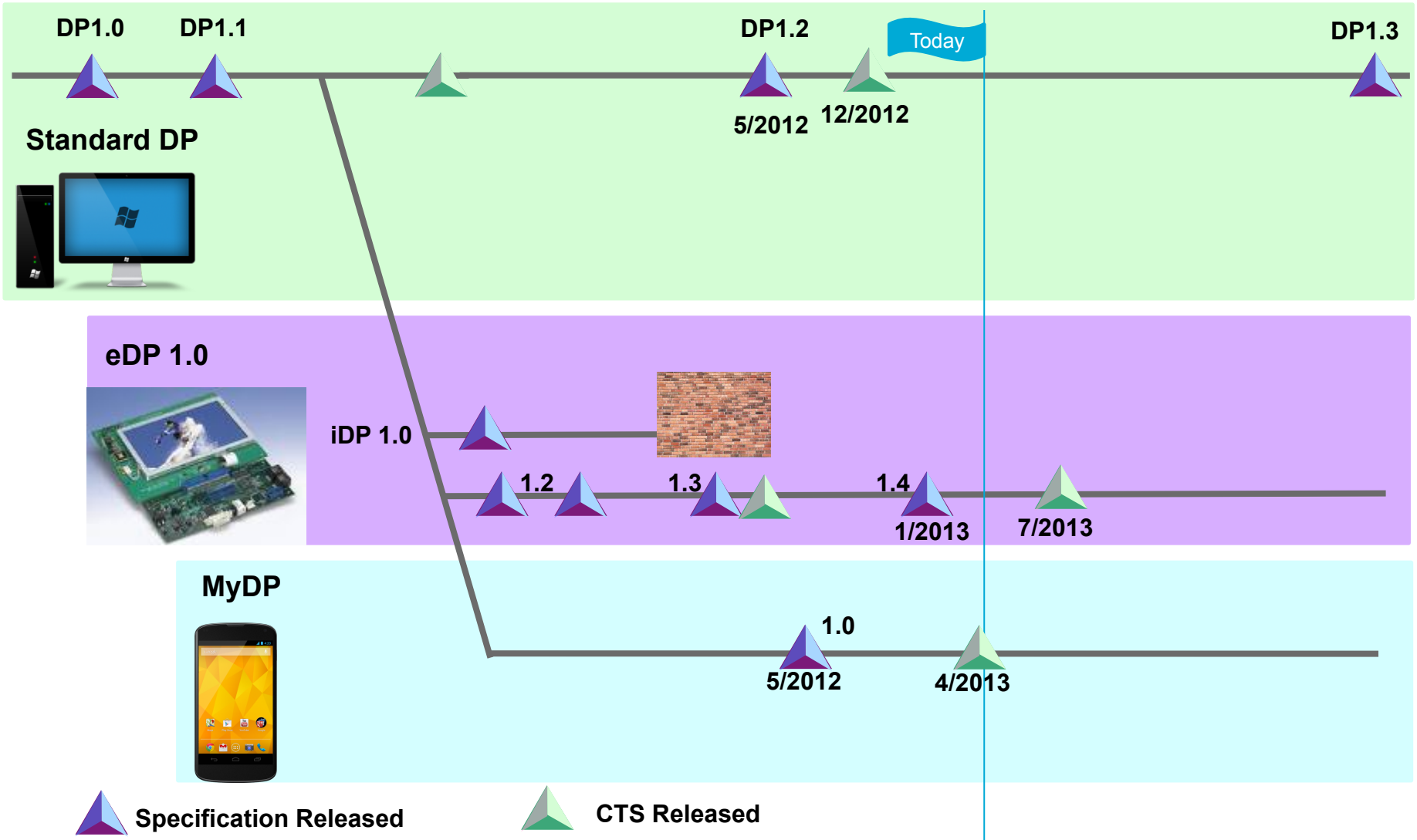
MyDP

Consumer Electronics

Portables

VESA: 200 members strong!

DisplayPort Technology Rollouts



Agilent Technologies

Confidentiality Label
May 10, 2013

Quick Summary

	Capabilities	Competing Technology	Noteworthy Features
Standard DisplayPort 	**1,2, or 4 lanes Four Settings for Lvl and Pre-emph SSC 3 bit rates**	**HDMI DVI? VGA?**	**Integrable in low geometry silicon. Dominating in PCs now.**
eDP 	**1,2, or 4 lanes Multi-Level Pre-emph SSC Multi bit rates**	**LVDS MIPI**	**Low Power rivals MIPI. High data rates supported now. Attributes similar to DP**
MyDP 	**1 lane Four Levels Pre-emphasis SSC 3 bit rates**	**MHL**	**1080p/60 24 bit color achieved. Many connection models. Attributes same as DP**

Why Successful?

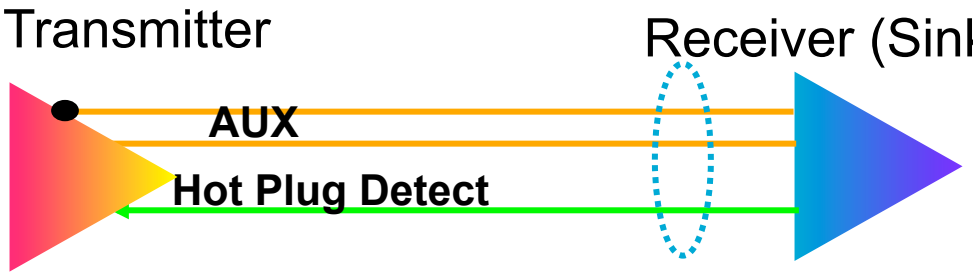
- ✓200 member companies participating
- ✓Original DP foundational principles serving DP extensions
- ✓Consumer focus in handling Legacy designs
- ✓Interoperability Program/Self testing/Compliance testing
- ✓Knowledgeable and Aggressive leaders

Craig Wiley
Parade Technologies

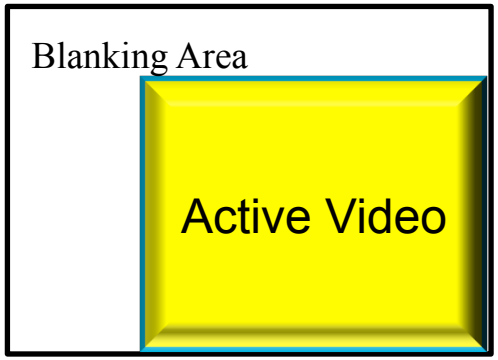
Alan Kobayashi
ST Micro

Key Features of DisplayPort

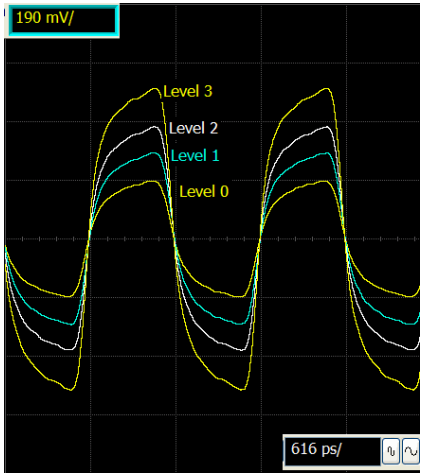
- **AUX Channel**
  - Very robust channel
  - Setup Link/Maintain Link
  - Test Assistance



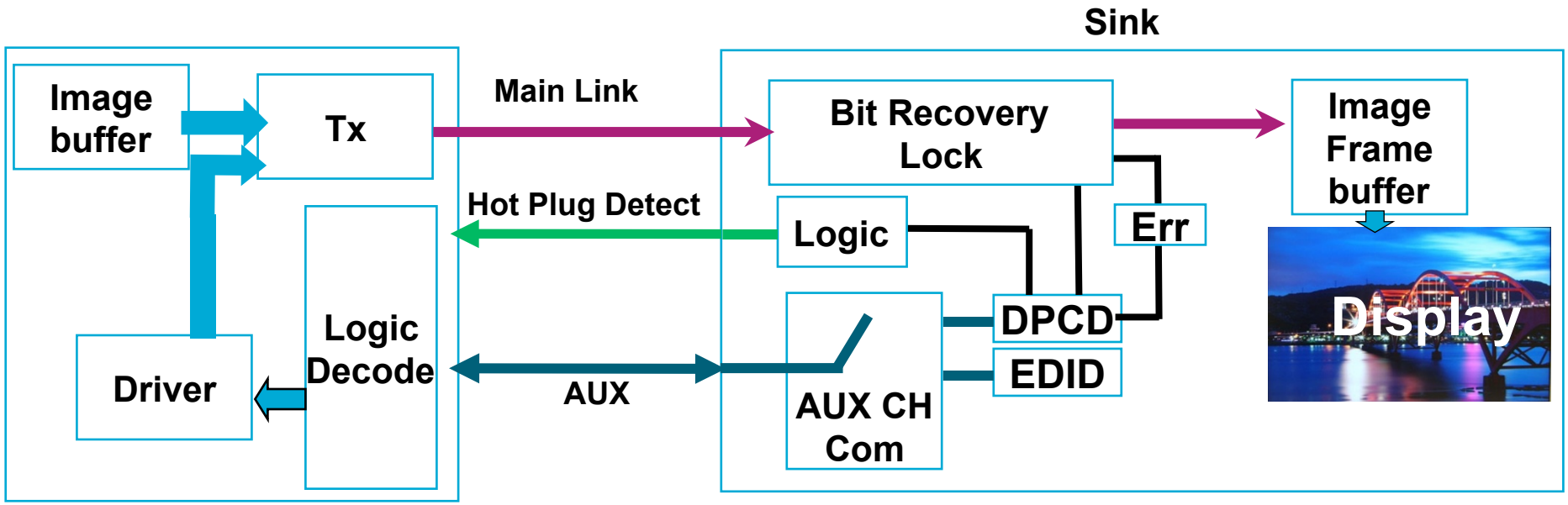
- **uPacket Based**
  - Not based on Raster timings
  - Fixed bit rates



- **Physical Layer Features**
  - Multiple Bit rates
  - Multiple Levels
  - Multiple Pre Emphasis Settings
  - Spread Spectrum Clocking



DisplayPort Link



The AUX Channel enables Link setup and maintenance as well as control for testing.

AUX Channel Implementation
Manchester II Signaling

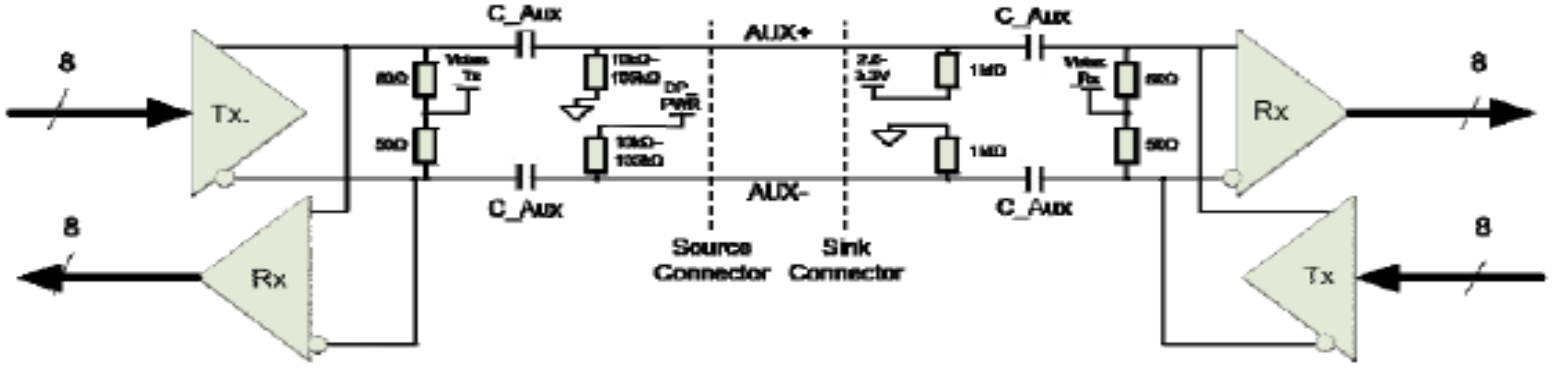


Figure 3-22: AUX CH Differential Pair

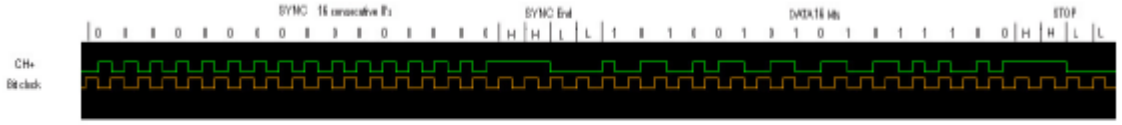


Figure 3-24: AUX CH SYNC Pattern and STOP Condition

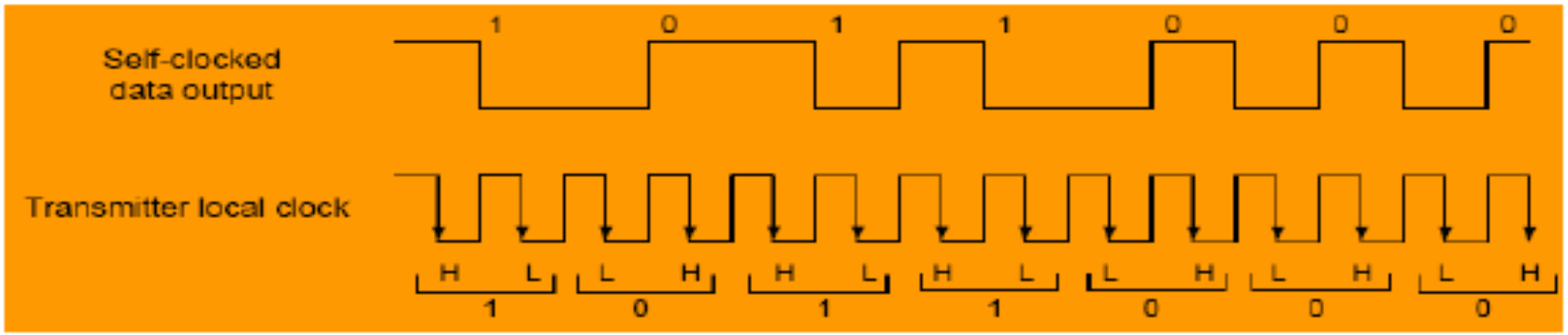


Figure 3-23: Self-clocking with Manchester-II Coding

MyDP: Portable →TV

Today:
MyDP Connectivity

In the Future:
Wireless from your portable

Your Entertainment System

My Entertainment System

Transmission Requirements

4k x 2k ?

No Way !
Not Yet Anyway

Using HDMI transmission as a benchmark…

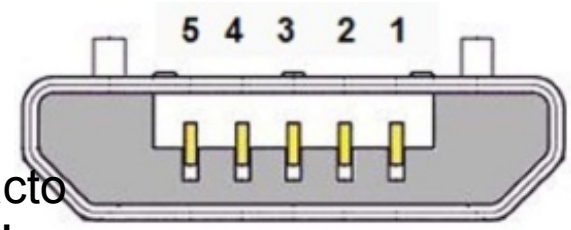
Timing	1080i/720p	1080p/8bit	1080p/10bit
Lane Bit Rate	750Mbs	1.50Gbs	1.87Gbs
Pixel Rate	75MPs	150MPs	187MPs
Composite Bit Rate	2.23Gbs	4.46Gbs	5.57Gbs

Display Technologies Available:

DisplayPort: Maximum Lane Rate--5.4Gbs

HDMI: Maximum Lane Rate----------3.4Gbs

Let's Look Closer…

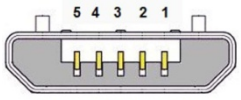


Micro USB Male connector

For both MHL and MyDP the uUSB connector is the de facto connector, but it is not find it mentioned in either standard!

MyDP does not specify either a connector type or a pin-out of a connector connecting a MyDP Source device to a MyDP-to-DP cable adaptor other than stating that it can be mapped to a connector with as few as five pins and that the electrical specification must be met at the MyDP connector pins as specified in Section 8 .

5 Pins



Micro USB Male connector

Pin	Name	Cable color	Description
1	VCC	Red	+5 VDC
2	D-	White	Data -
3	D+	Green	Data +
4	ID		Mode Detect. May be N/C, GND or used as an attached device presence indicator (shorted to GND with resistor)
5	GND	Black	Ground

⇦ D- and D+ is the differential data lane

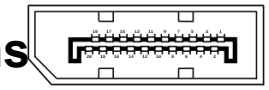
⇦ ID: USB mode detect

Conclusion: There is only one data lane through which the composite data rate must be conveyed. So the composite bit rate rate is the metric.

Getting down to One data lane…

DisplayPort

20 Pins



Pin Number	Signal Type	Pin Name	Mating Row Contact Location
1	In	ML_Lane 3(n)	Top
2	GND	GND	Bottom
3	In	ML_Lane 3 (p)	Top
4	In	ML_Lane 2 (n)	Bottom
5	GND	GND	Top
6	In	ML_Lane 2 (p)	Bottom
7	In	ML_Lane 1 (n)	Top
8	GND	GND	Bottom
9	In	ML_Lane 1 (p)	Top
10	In	ML_Lane 0 (n)	Bottom
11	GND	GND	Top
12	In	ML_Lane 0 (p)	Bottom
13	CONFIG (see note 1)	CONFIG1	Top
14	CONFIG (see note 1)	CONFIG2	Bottom
15	I/O	AUX CH (p)	Top
16	GND	GND	Bottom
17	I/O	AUX CH (n)	Top
18	Out	Hot Plug Detect	Bottom
19	RTN	Return	Top
20	Power Out (see note 2)	DP_PWR	Bottom

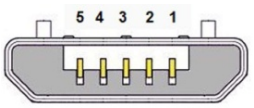
For Use Only

AUX+/-, HPD
Config1/2

4 data lanes

Power, Ground

5 Pins



Micro USB Male connector

1 data lane

1 low speed line

Power, Ground

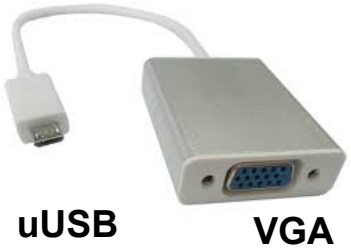
MyDP

MyDP

Spec Released: 1.0

Compliance Testing starting: June 2013

Maximum Data Rate: 5.4Gbs to support 1080p/60Hz



MyDP

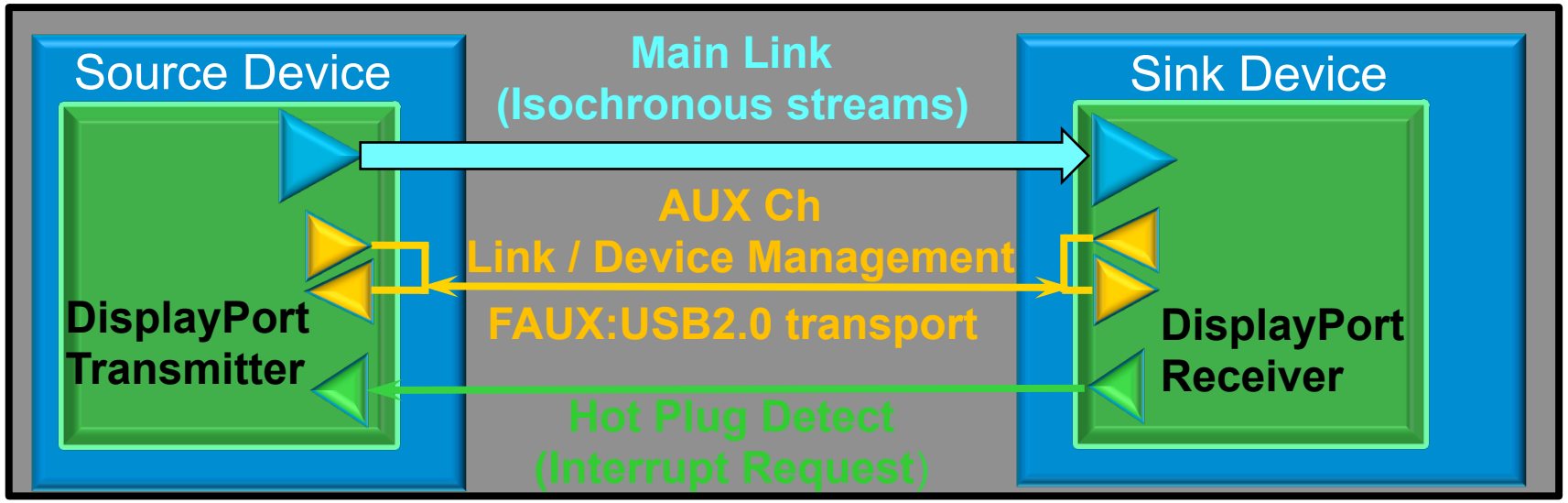
- One could say that MyDP is not very new!

  It is just one lane DisplayPort!

- There are other changes to get to 5 pin interface, but nothing changes in the high speed signaling.

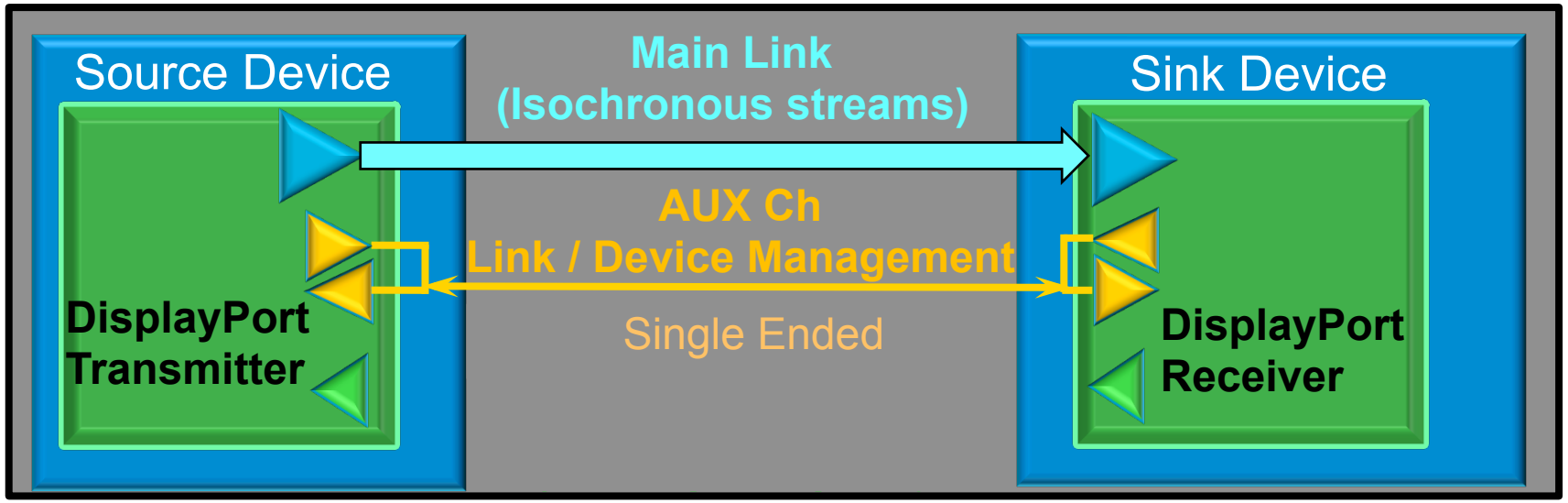
- Subsequent slides will be paired; the first to show the standard DisplayPort attributes and the next those for MyDP.

DisplayPort Technology



- ❑ 1 to 4 unidirectional high speed lanes
  - – Fixed data rate independent of display raster (refresh)
- ❑ Auxiliary channel for link communication and auxiliary data flow
  - Link Setup and Maintenance (1Mb/s - Manchester II)
  - USB 2.0 Transport (Fast AUX -540Mb/s - standard 8b/10b)
- ❑ Auto detect of cable plug/unplug

MyDP Technology



- ❑ 1 unidirectional high speed lane
  - – Fixed data rate independent of display raster (refresh)
- ❑ Auxiliary channel for link communication and auxiliary data flow
  - Link Setup and Maintenance (1Mb/s - Manchester II)
  - Single Ended
- ❑ Polling detect of cable plug/unplug

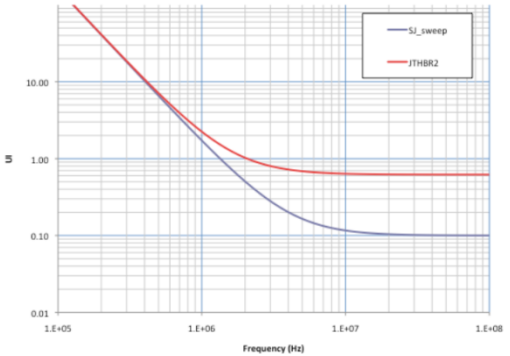
DP Technology: Specifications

Silicon structures:

- Structure leveraged from PCI Express
- Implementable on sub 65nm process
- Termination Voltage must be <2volts (internal to IC)

Receiver

- PLL BW=10MHz effective.
  Jitter tolerance curve specified.



Data Rate

- 1.62 Gbs (RBR)
- 2.7 Gbs (HBR) [units supporting HBR must support RBR]
- 5.4Gbs (HBR2) [units supporting HBR2 must support HBR]

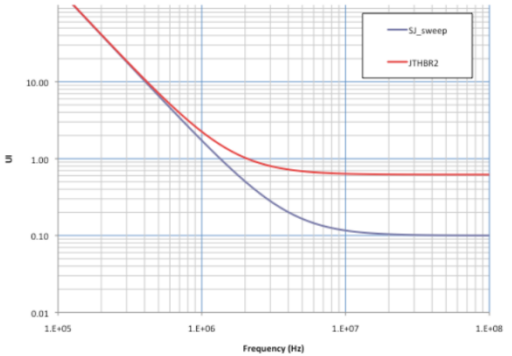
MyDP Technology: Specifications

Silicon structures:

- Structure leveraged from PCI Express
- Implementable on sub 65nm process
- Termination Voltage must be <2volts (internal to IC)

Receiver

- PLL BW=10MHz effective.
  Jitter tolerance curve specified.



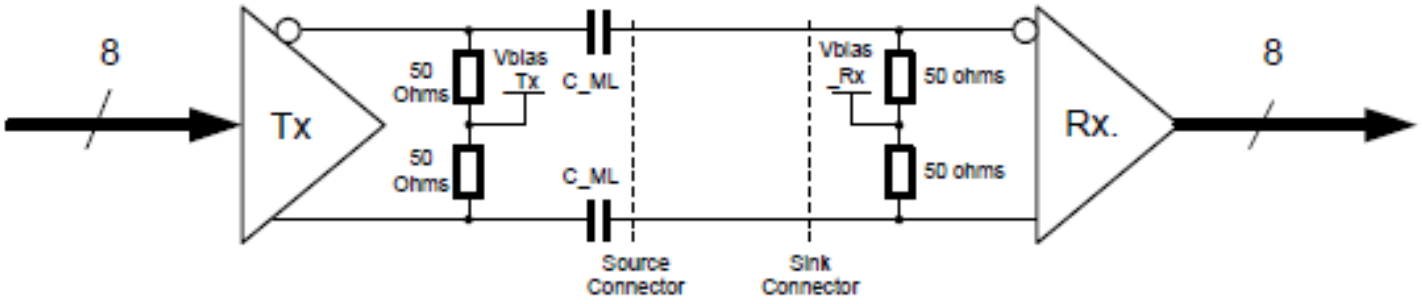
Data Rate

- 1.62 Gbs (RBR)
- 2.7 Gbs (HBR)
- 5.4Gbs (HBR2)

DP Technology: Main Link Lanes

Lanes

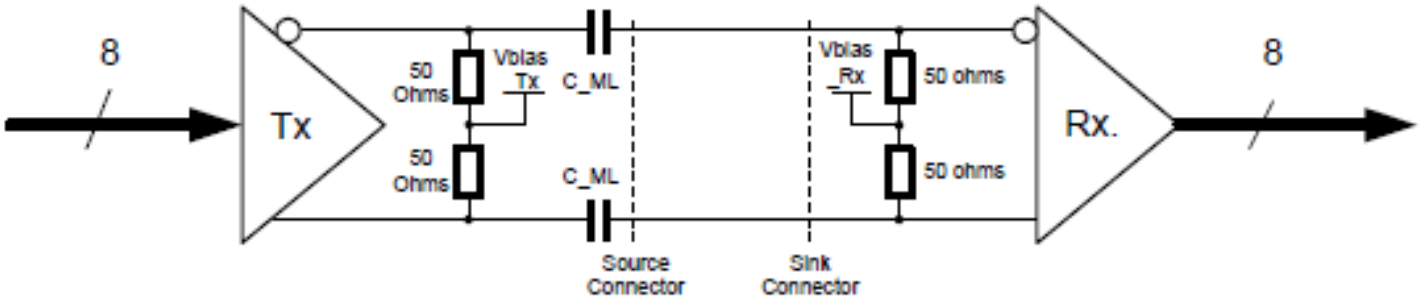
- Each lane is Differential, 100Ω.
- 1, 2, 4 lane models for video data transport. 4 lane model capable must support 1 & 2 lane models. 2 lane model must support 1 lane model. Lanes are uni-directional.
- ANSII standard 8b/10b.
- Each lane has separate clock recovery from its data. No Explicit Clock.
- Single ended lines of each lane are source and sink terminated and biased. No external pull-up is needed for test equipment.



MyDP Technology: Main Link Lane

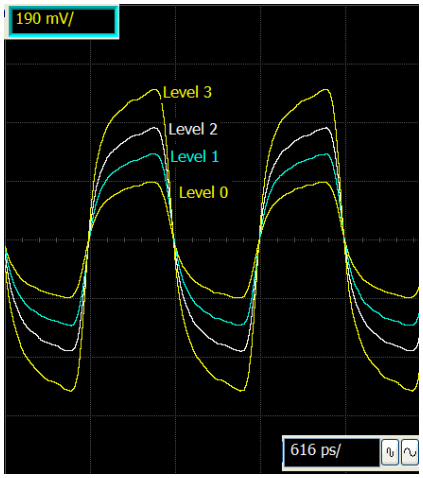
Lanes

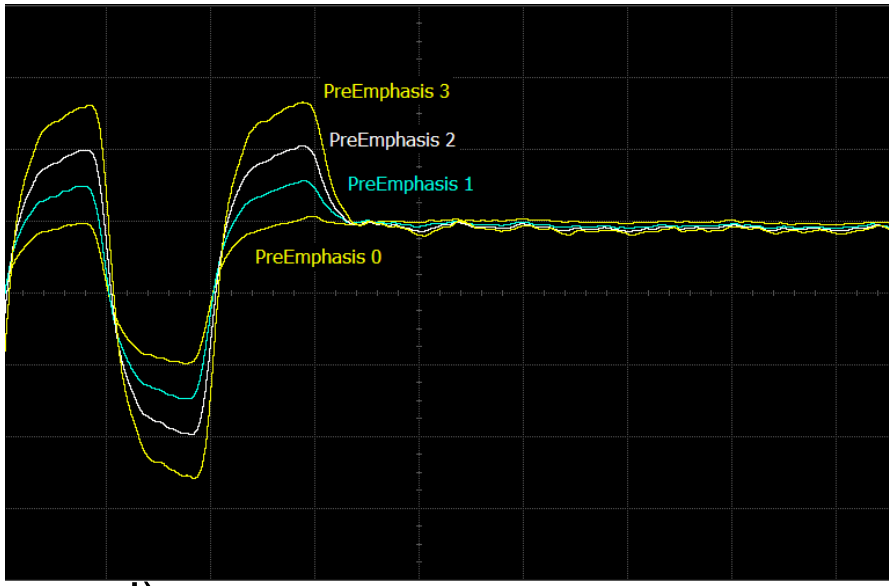
- Each lane is Differential, 100Ω.
- 1 lane for video data transport. Lane is uni-directional.
- ANSII standard 8b/10b.
- Clock recovery from the data.
- Single ended lines of each lane are source and sink terminated and biased. No external pull-up is needed for test equipment.



DP Technology: Signal Attributes

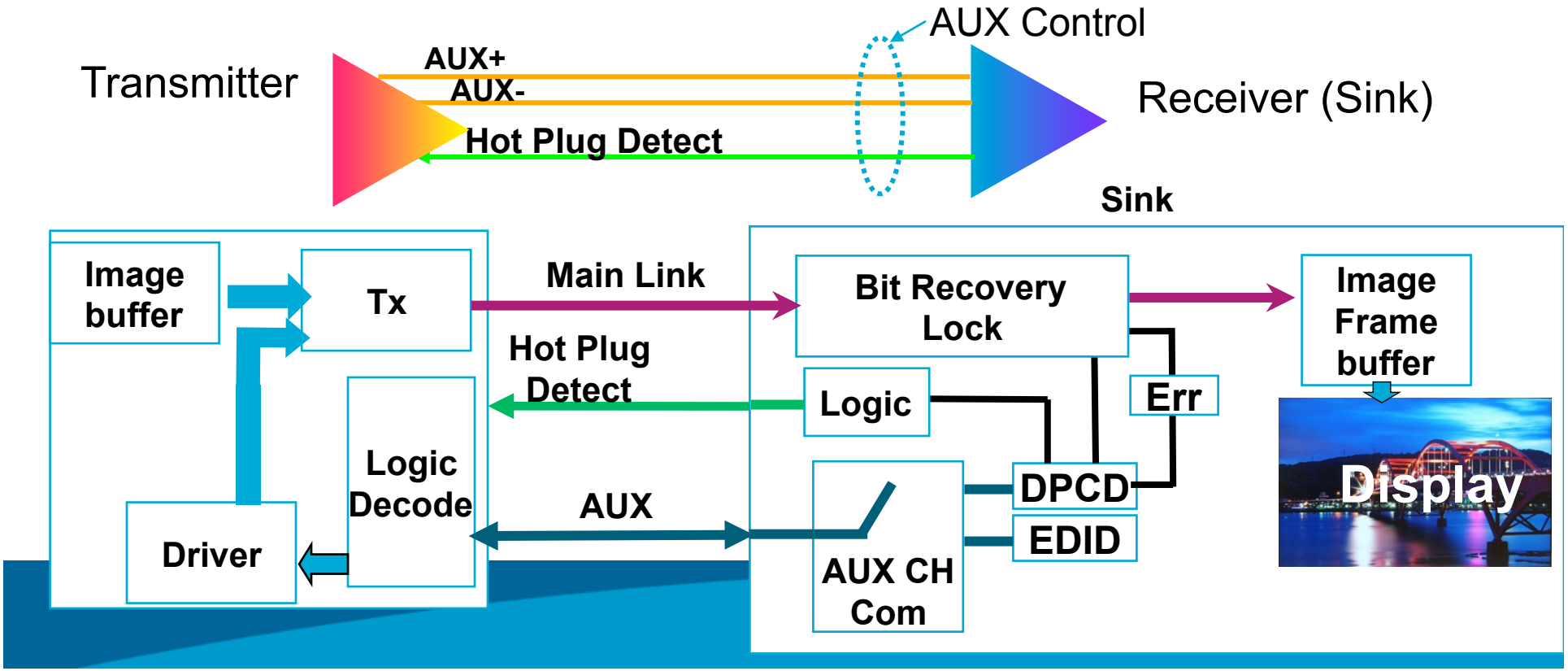
- Four swing settings:
  Setting 0: 400mV nominal
  Setting 1: 600 mV nominal
  Setting 2: 800 mV nominal
  Setting 3: 1200 mV nominal (optional)
- Four Pre-Emphasis settings
  Setting 0: 0 dB nominal
  Setting 1: 3.5 dB nominal
  Setting 2: 6 dB nominal
  Setting 3: 9.5 dB nominal (optional)
  Compliance Test Specification emphasizes monotonicity not accuracy
- No combination of voltage and pre-emphasis can exceed 1200mVolts p-p
- Spread Spectrum Clocking
  (30-33KHz spreading frequency,downspread)





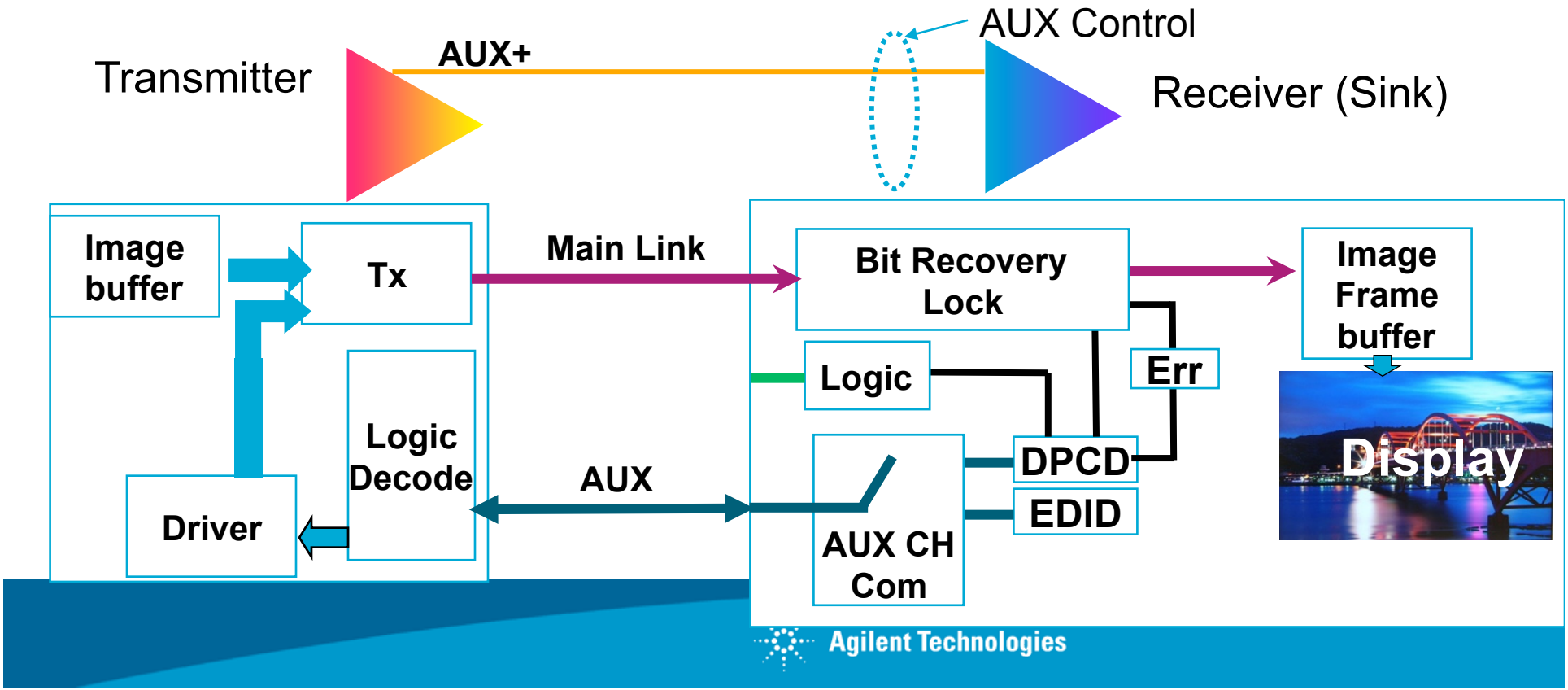
DP Technology: AUX Channel, DPCD

- Designated Control Link lane called ‘the AUX Channel’ specified. Operates at 1Mbs and is used in Link Training and Link Management and is Bidirectional Half Duplex.
- The Transmitter is the master.
- Receiver gains attention by pulling down on the Hot Plug Detect line.
- Manchester II coding (shown subsequently)



MyDP: AUX Channel, DPCD

- Designated Control Link lane called 'the AUX Channel' specified. Operates at 1Mbs and is used in Link Training and Link Management and is Bidirectional Half Duplex.
- The Transmitter is the master.
- Receiver identified by polling. Link serviced by occasional DPCD reads.
- Manchester II coding (shown next page)



DP AUX Channel Implementation
Manchester II Signaling

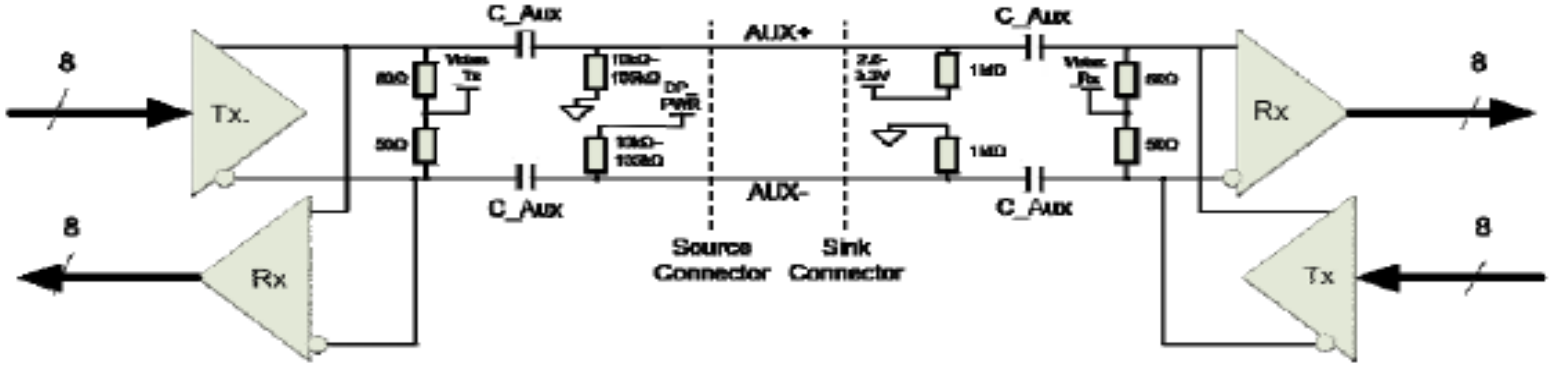


Figure 3-22: AUX CH Differential Pair

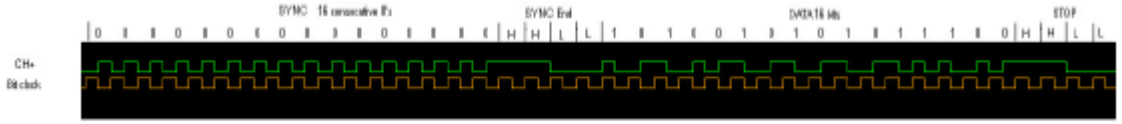


Figure 3-24: AUX CH SYNC Pattern and STOP Condition

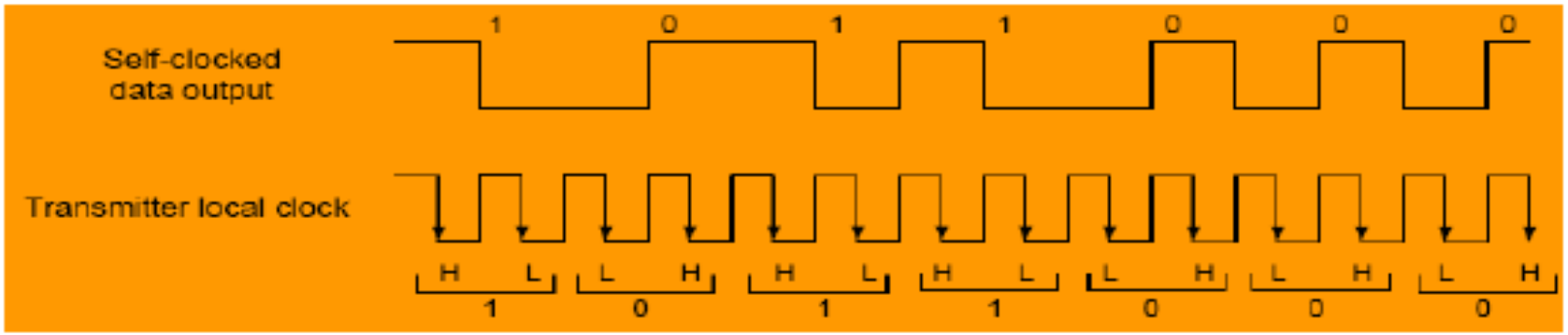


Figure 3-23: Self-clocking with Manchester-II Coding

MyDP AUX Channel Implementation
Manchester II Signaling, Single Ended

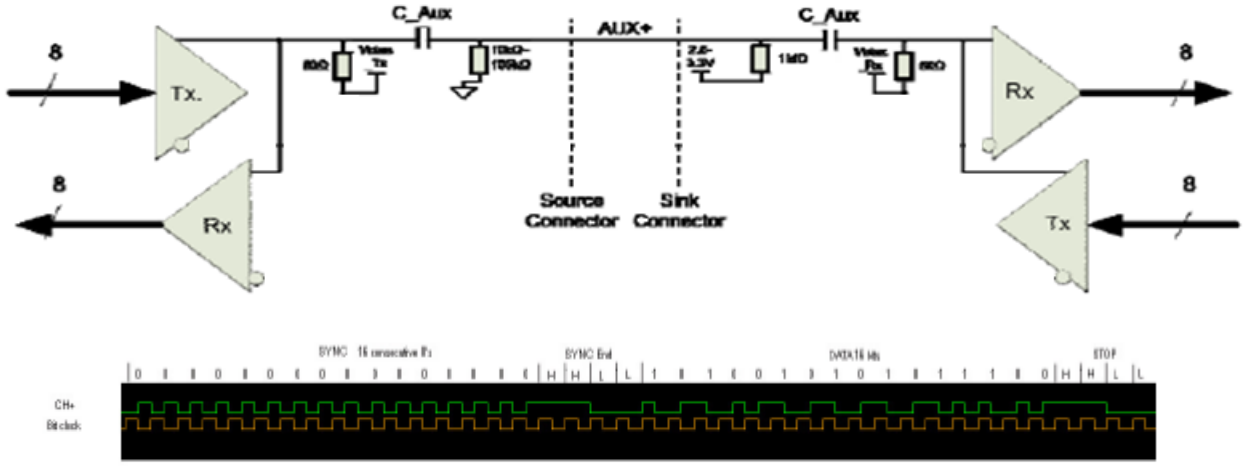


Figure 3-24: AUX CH SYNC Pattern and STOP Condition

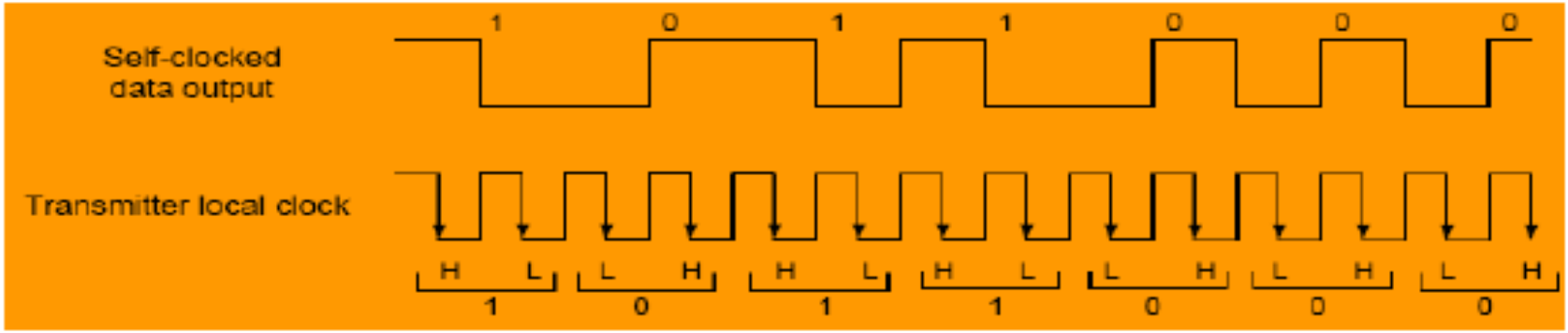
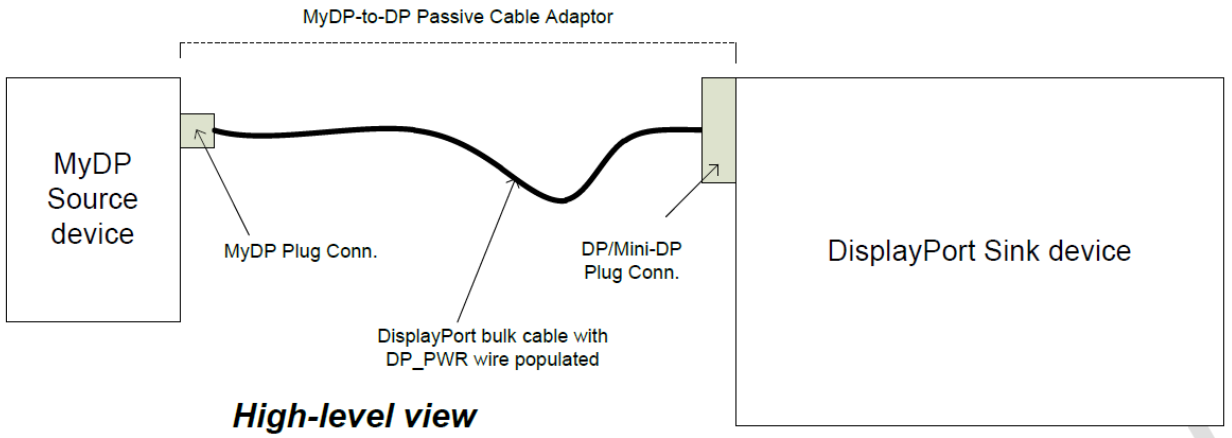
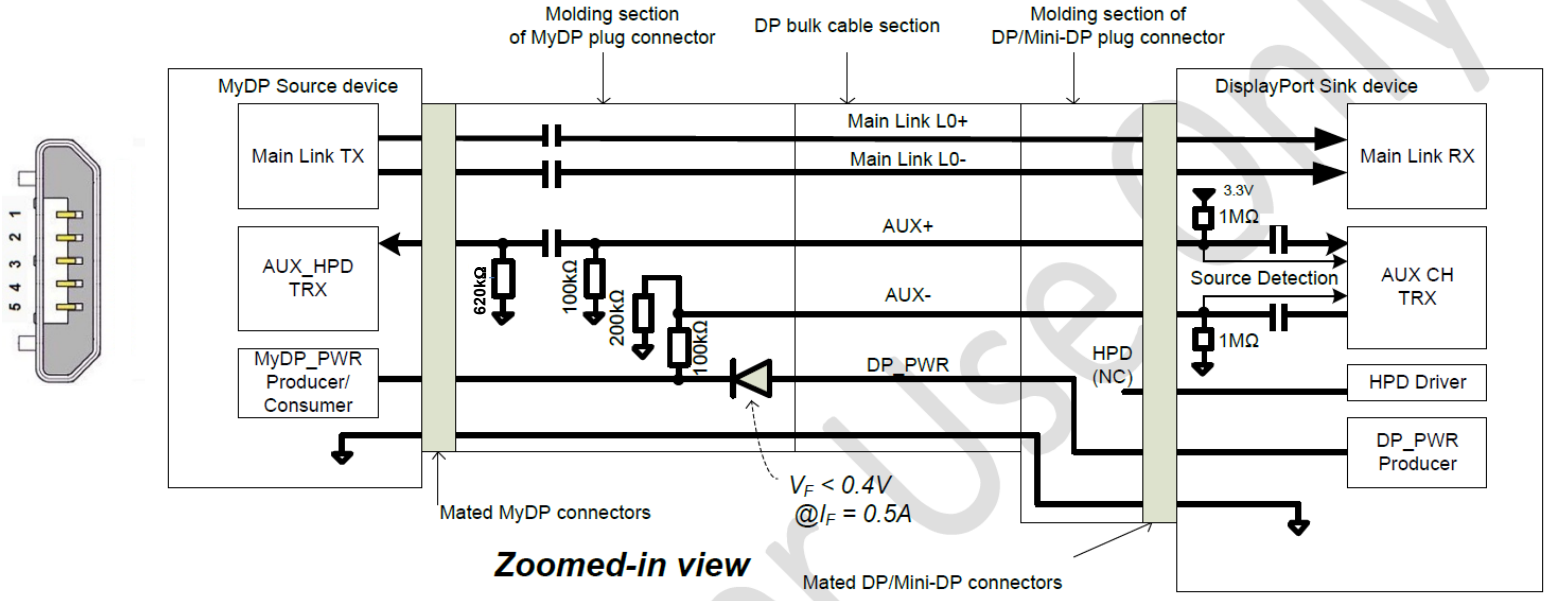


Figure 3-23: Self-clocking with Manchester-II Coding

MyDP connection requirements.



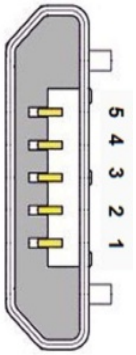
High-level view



Zoomed-in view

For Use Only

Testing MyDP



Gnd
AUX-HPD
D-
D+
Pwr

MyDP Transmitters

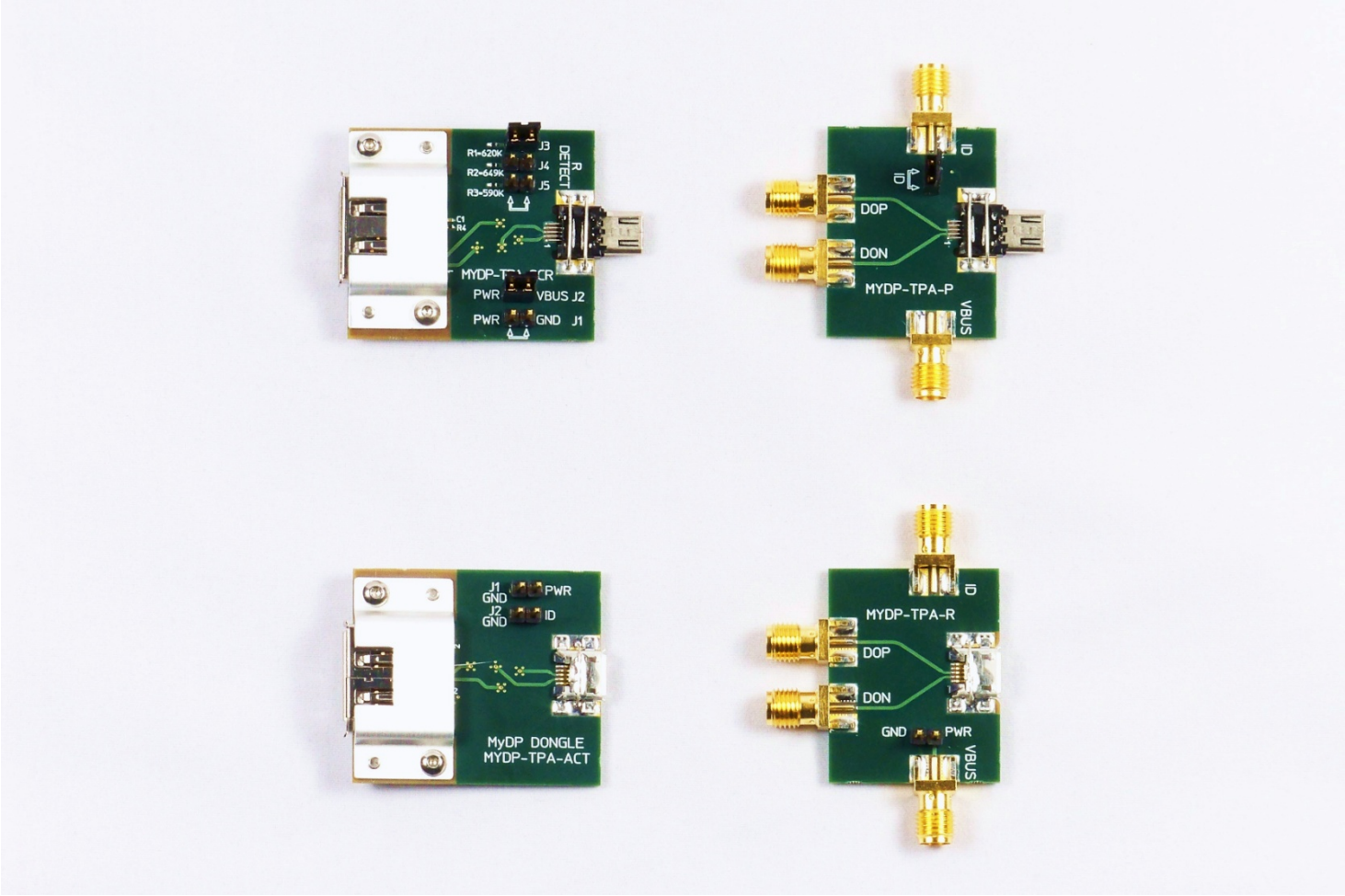
✓AUX-HPD
✓Power Charging
✓Waveform Parametrics
✓Video/Audio Protocol Validation

MyDP Receivers

DisplayPort!
✓Power Charging
✓Video/Audio Protocol Response
✓Receiver Sensitivity/Jitter Tolerance
(using test mode BER counting)

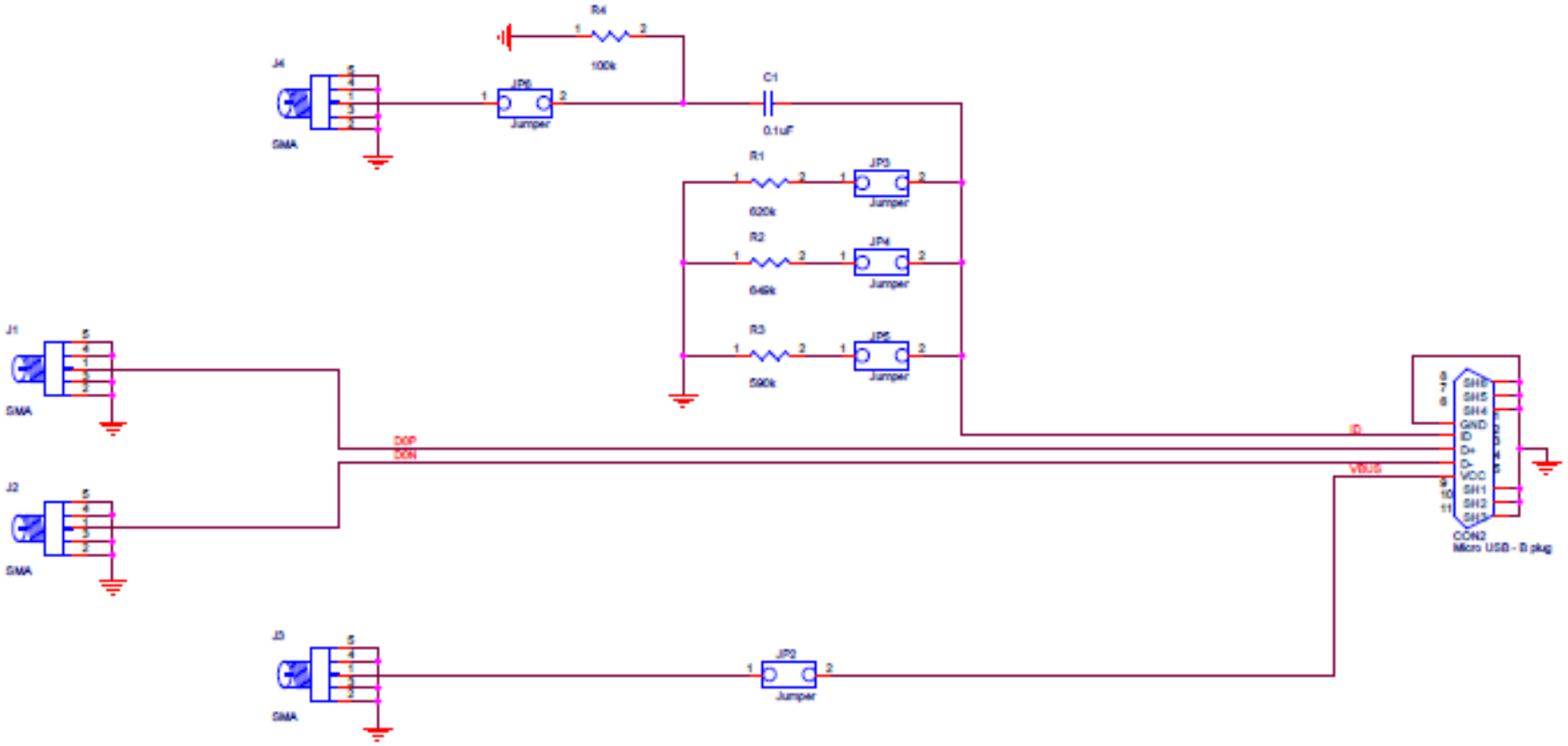
Test Fixtures

These are the MyDP fixtures from Wilder Technologies. .

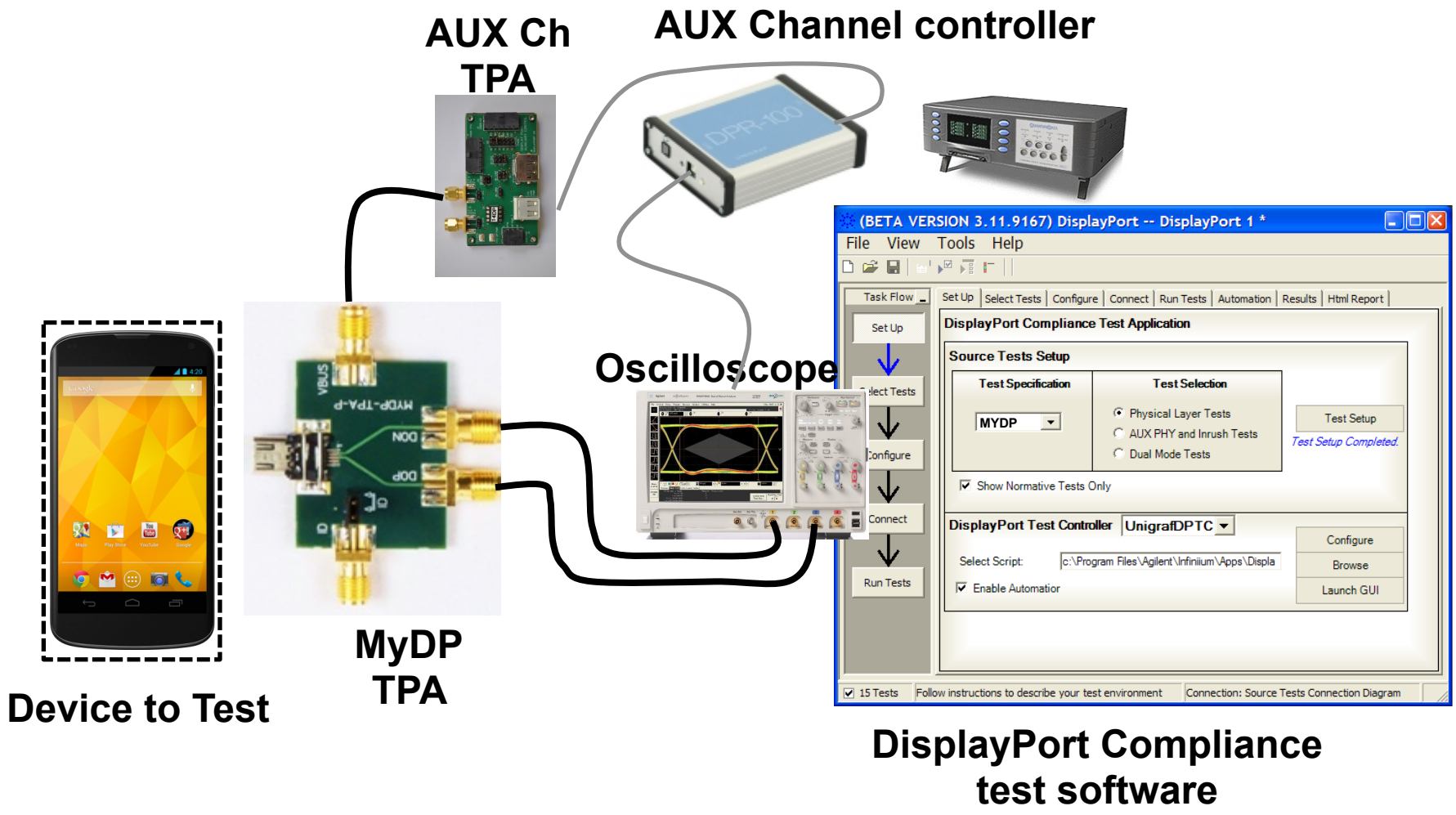


MyDP Fixture Schematic

From Wilder:



MyDP Source Testing

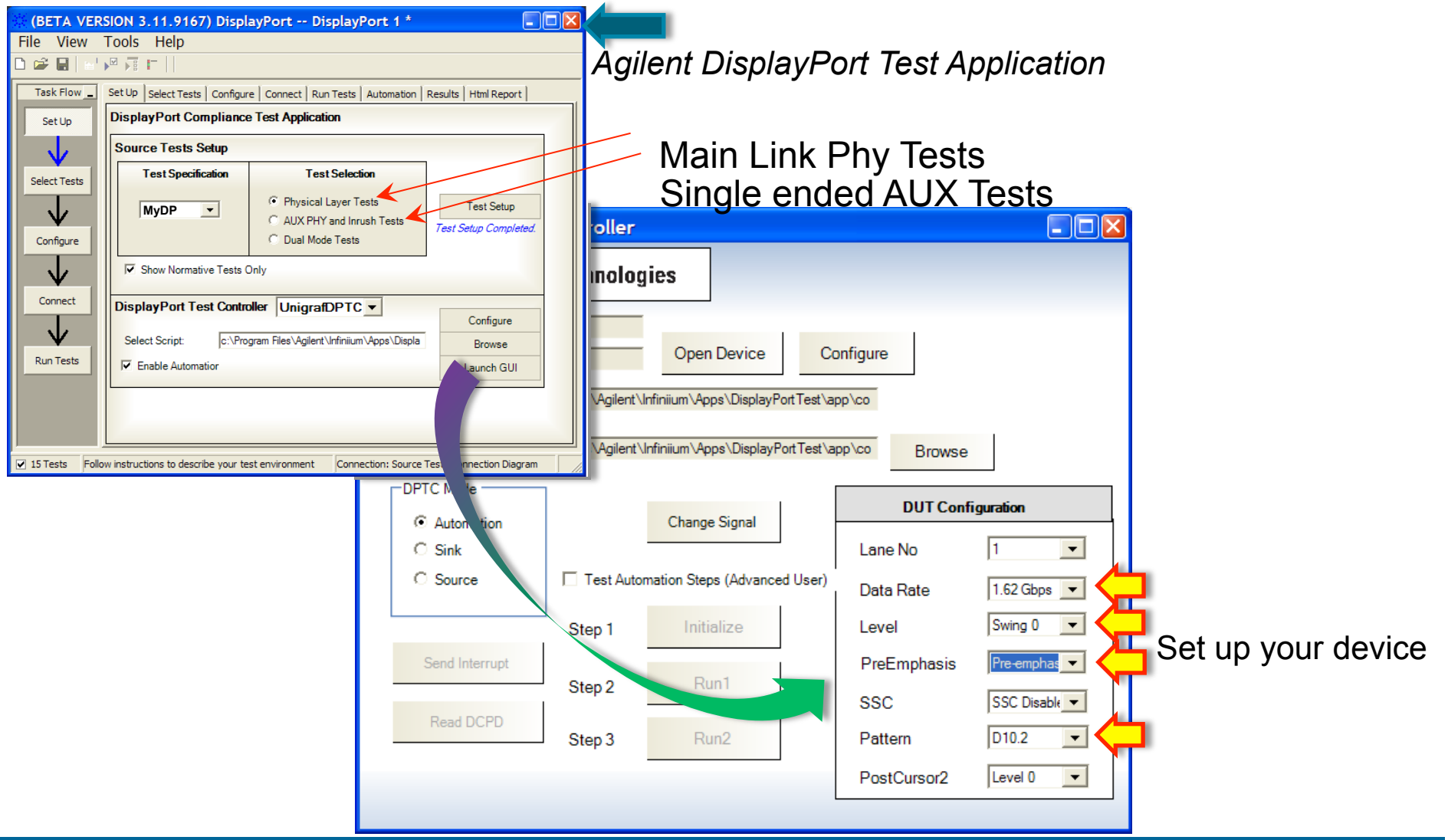


The test suite for standard DP applies for MyDP

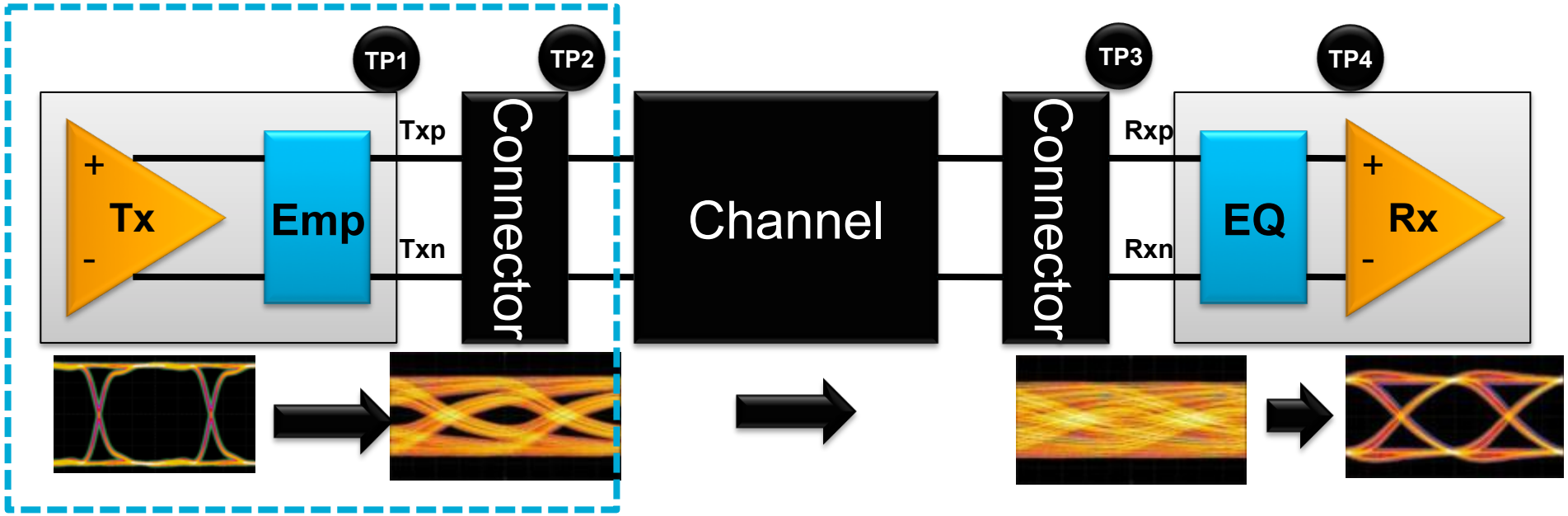
Preparing for Test

Control of your MyDP Device

CONTROL



PHY Source Tests



MyDP source testing is at TP2 only

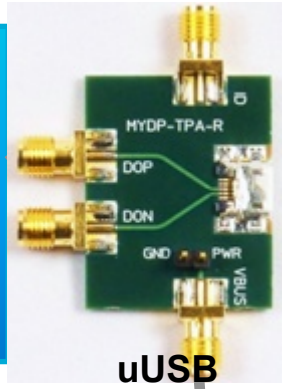
Eye Diagram	Jitter: Non ISI,Total Jitter,HBR2 RJ/DJ/TJ
Non Pre-Emph Level	Main Link Frequency
Pre-Emphasis Level	AUX Eye
Intra Pair Skew	AUX Sensitivity

MyDP Sink Testing

MyDP ‘Sink’ Calibration and Test

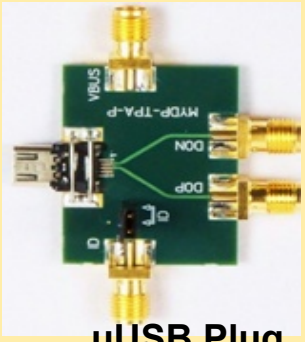
Test Equipment

Signal Conditioning

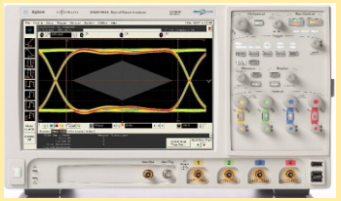


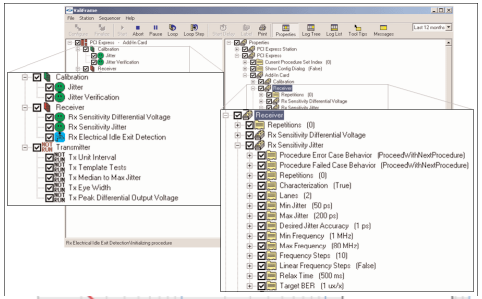
uUSB Receptacle

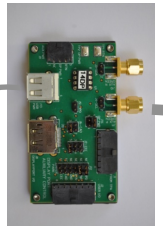
Calibration

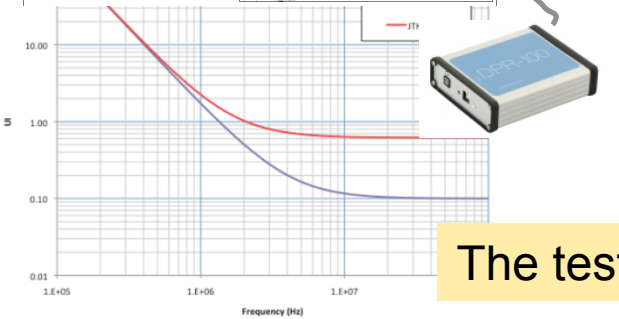


uUSB Plug









Test

Dongle

uUSB PLUG

VGA

DVI

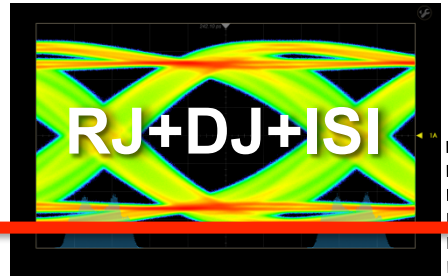
HDMI

DP

The test suite for standard DP applies for MyDP. Specs are different

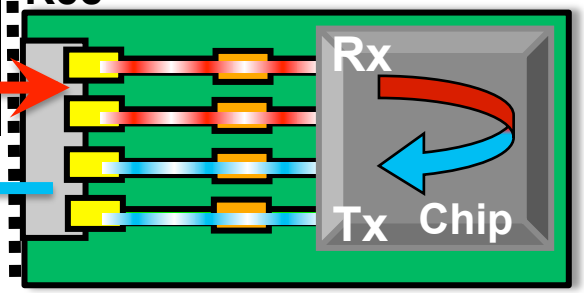
Sink Test Jitter Components (RJ+DJ +ISI)

N4903B JBERT

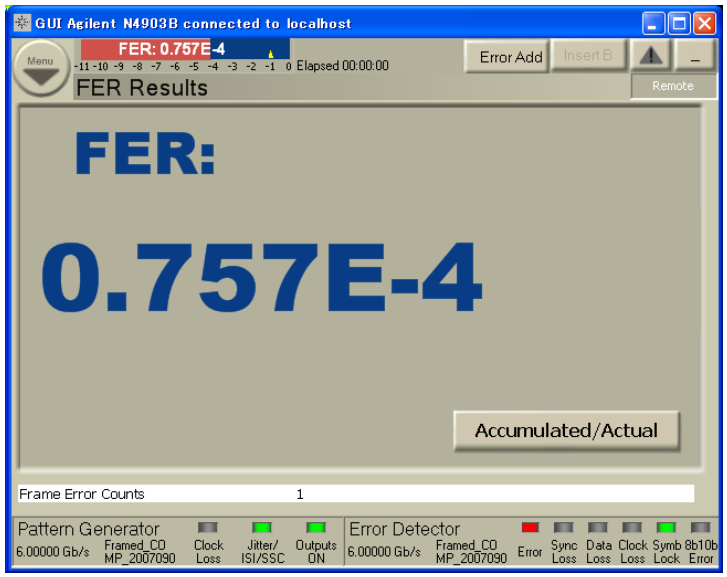


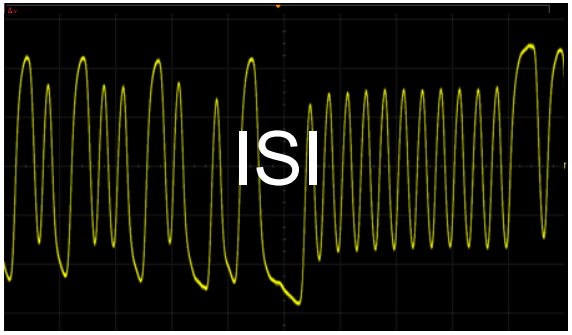
Sink Device

Loop Back



Error Detection





Summary of MyDP

MyDP is merely 1 lane DP so no modifications on the main link or protocol. Only significant change is that the AUX lane is Single ended, and therefore, the AUX sensitivity is halved.

MyDP can do 1080p/60 with 24 bits of color.

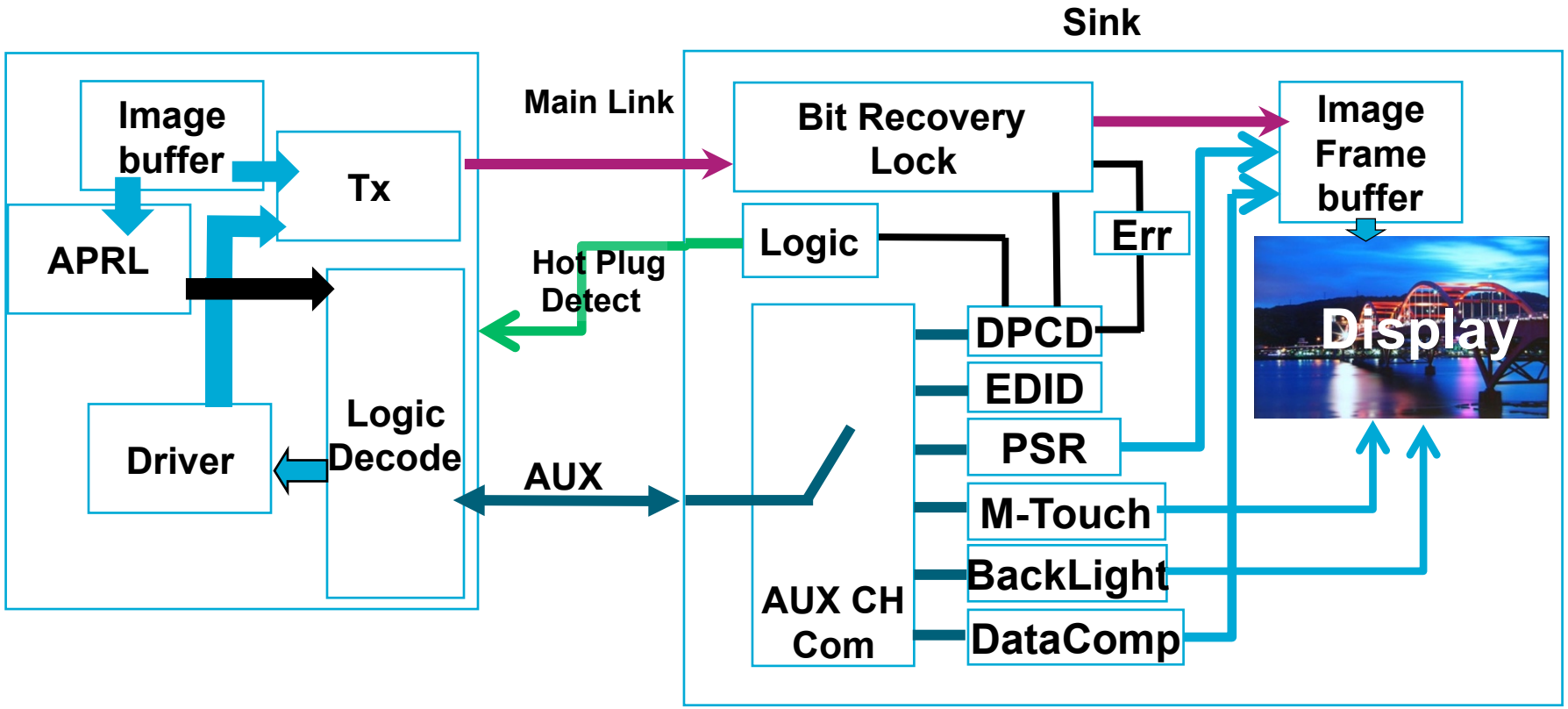
Same Connector, uUSB as MHL. Nothing else in common!

eDP1.4

Huge changes from eDP 1.3

Attribute	eDP 1.3	eDP1.4
Levels	4 (std DP)	6 (200mv-450mV) Arbitrary allowed
Bit Rates	3 (std DP)	7 (1.45 to 5.4Gbs) Arbitrary allowed
Pre-Emphasis	4 (std DP)	Arbitrary
Panel Self Refresh	Whole frame only	Partial Frame enabled
Compression	No	Yes
Multi-touch	No	Yes
BackLight control	Yes	Yes Regional control as well

AUX Channel Extended



Levels/PreEmphasis/BitRates

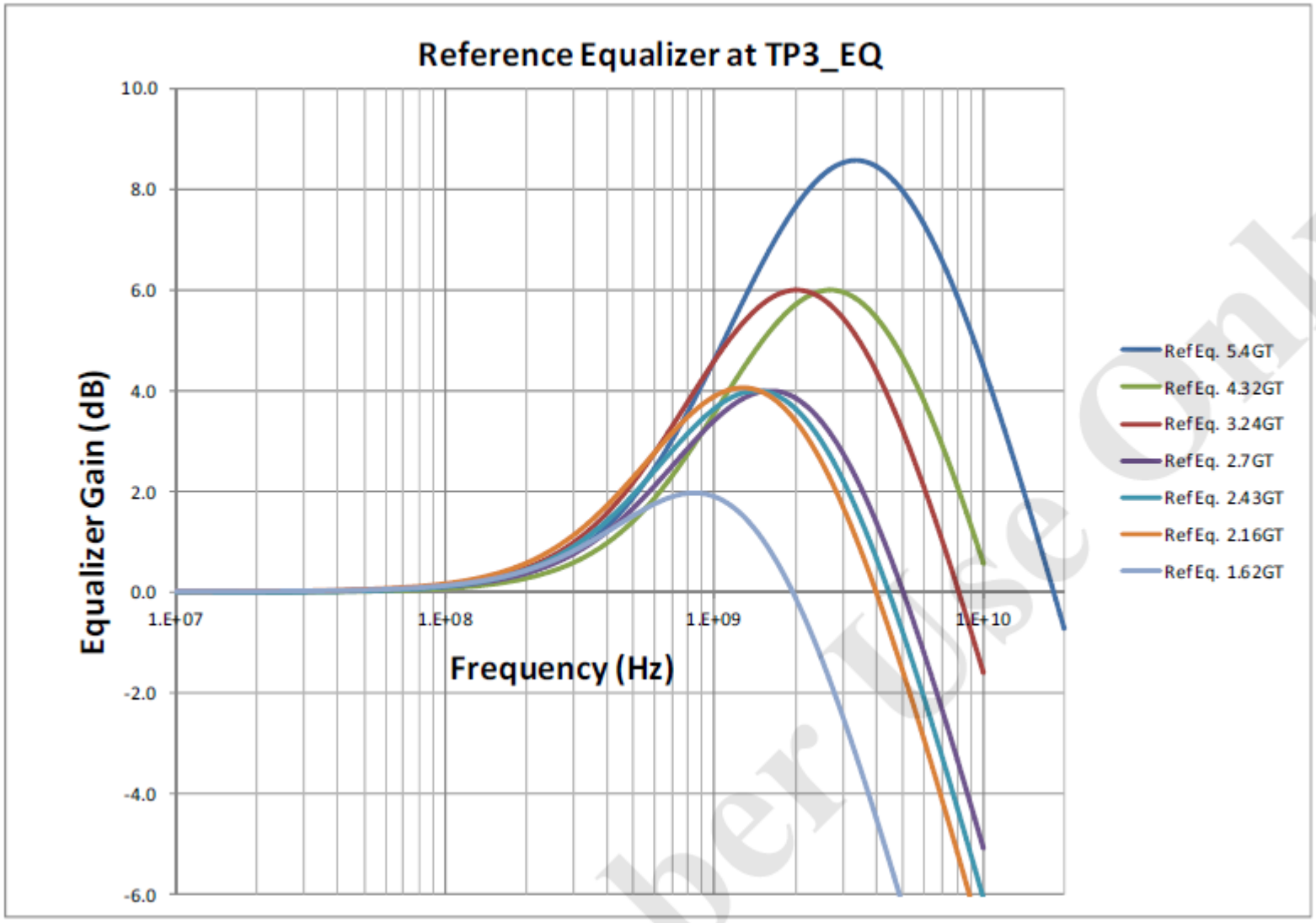
Link Rate Name	Parameter (Per Lane)	Nominal Per-lane Transfer Rate (Gbps/Lane)	Nominal Unit Interval (ps)
R162 (RBR)	Transfer Rate 1	1.62	617
R216	Transfer Rate 2	2.16	463
R243	Transfer Rate 3	2.43	412
R270 (HBR)	Transfer Rate 4	2.7	370
R324	Transfer Rate 5	3.24	309
R432	Transfer Rate 6	4.32	231
R540 (HBR2)	Transfer Rate 7	5.4	185

Non-transition $Vdiff_{P-P}$	Transition $Vdiff_{P-P}$			
	Training Pre-emphasis 0	Training Pre-emphasis 1	Training Pre-emphasis 2	Training Pre-emphasis 3
200mV	200mV	250mV	300mV	350mV
250mV	250mV	300mV	350mV	Unused
300mV	300mV	350mV	Unused	Unused
350mV	350mV	Unused	Unused	Unused

Non-transition $Vdiff_{P-P}$	Transition $Vdiff_{P-P}$			
	Training Pre-emphasis 0	Training Pre-emphasis 1	Training Pre-emphasis 2	Training Pre-emphasis 3
300mV	300mV	350mV	400mV	450mV
350mV	350mV	400mV	450mV	Unused
400mV	400mV	450mV	Unused	Unused
450mV	450mV	Unused	Unused	Unused

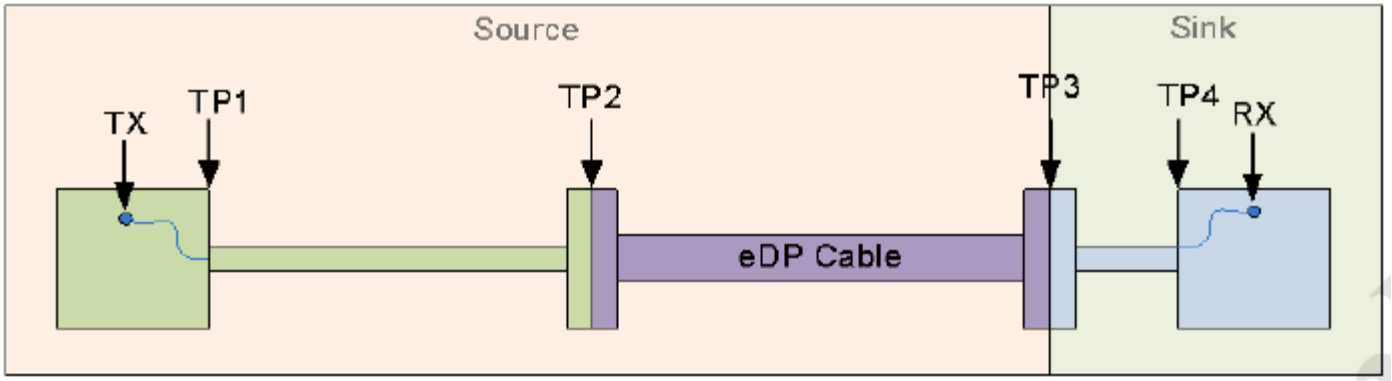
PAVMember

Reference Equalizers (for measurements only)

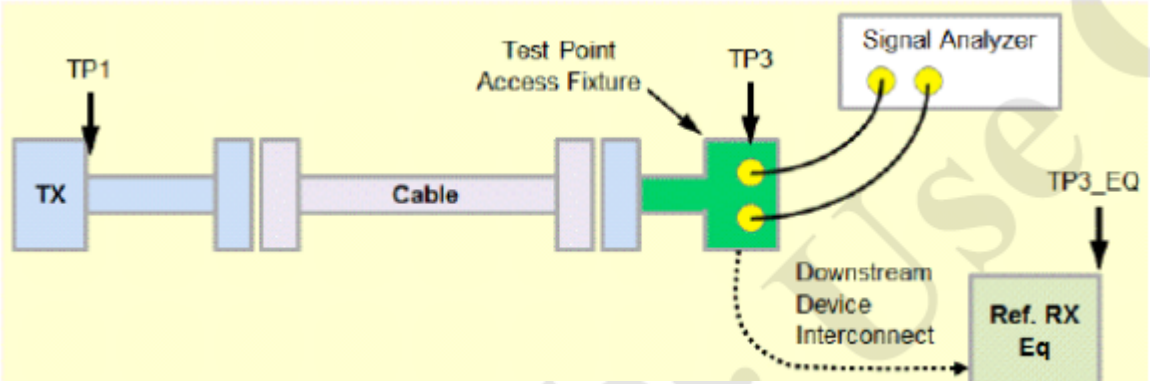


Agilent Technologies

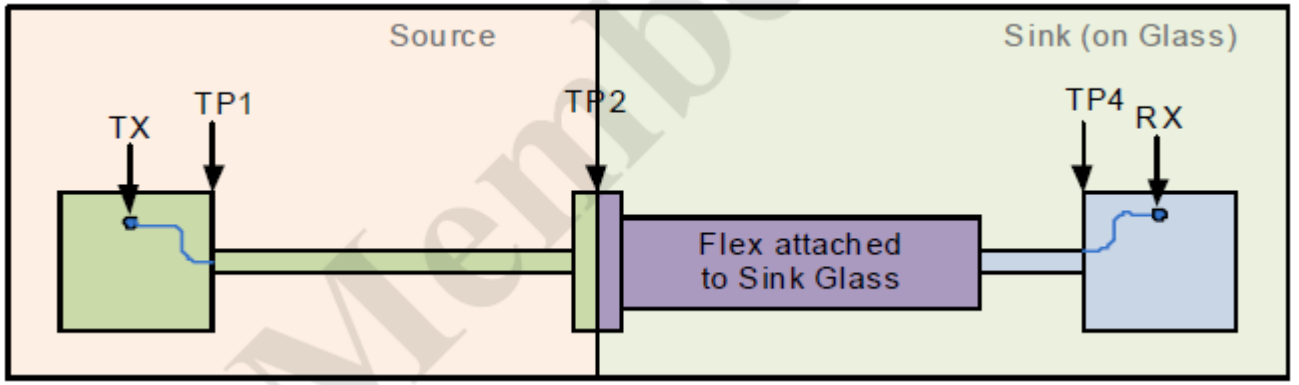
Test Points Available



eDP Test Point.



Test Fixture &Test Model



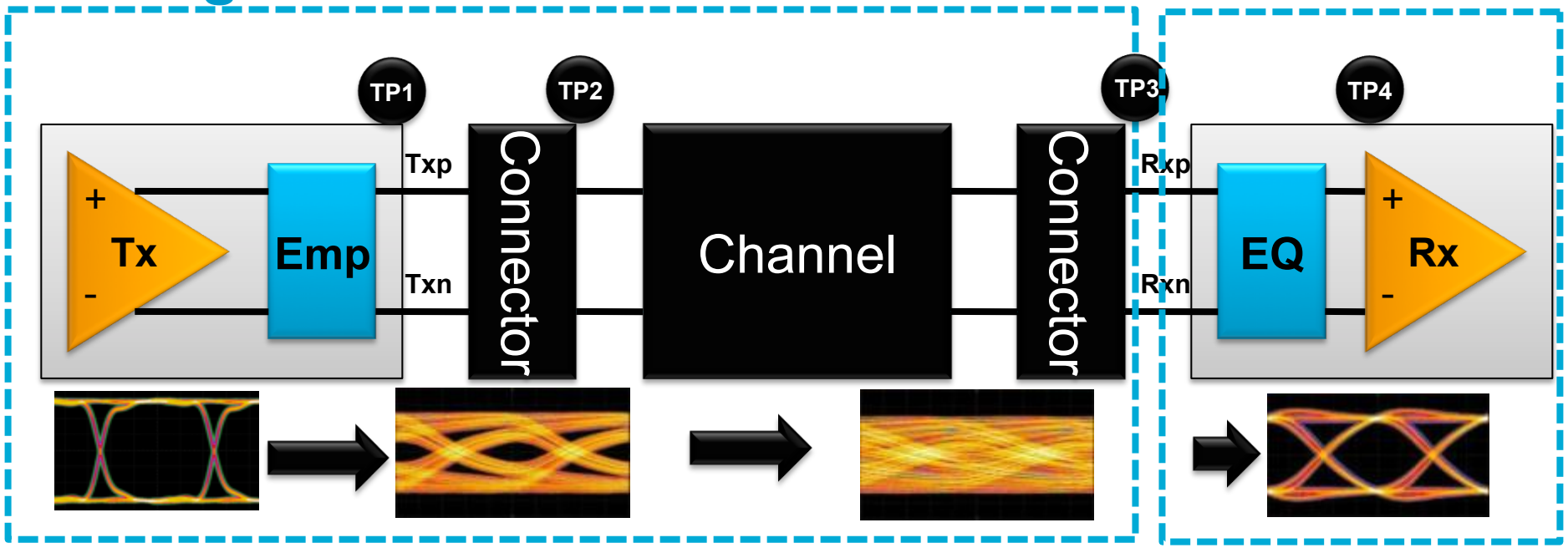
Test at a Modified TP2.

Member Use

Testing eDP

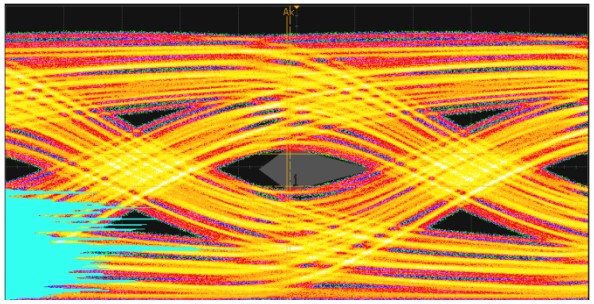
1. Lots of bit rates and levels and arbitrary settings are allowed.
2. TestPoint is TP3, the cable is considered part of the source
3. A Test guideline is being created now. Mike Hamann of Intel is leading this effort.
   VESA® eDP1.4 PHY Compliance Test Guideline, Version 1.0
   OPEN ISSUES:
   HBR2 Pattern CP2520,
   Data Rate Measurement (SSC),
   TX AUX Channel Eye Derivation
   RX AUX Over-Sampling Assumptions

Testing eDP

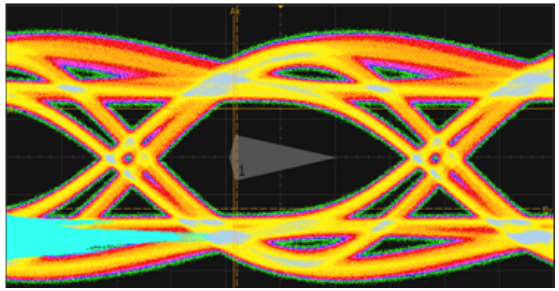


eDP source testing is at TP3 only. Equalizers need to be applied to overcome losses of channel generally.

eDP sink evaluation is typical TP3 testing.

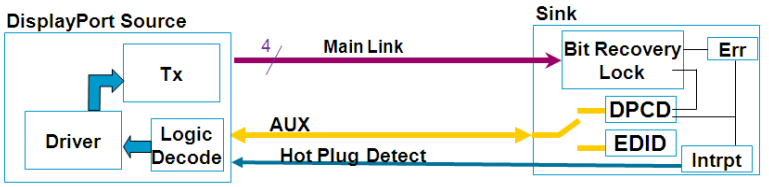


Eye after Channel (TP3)

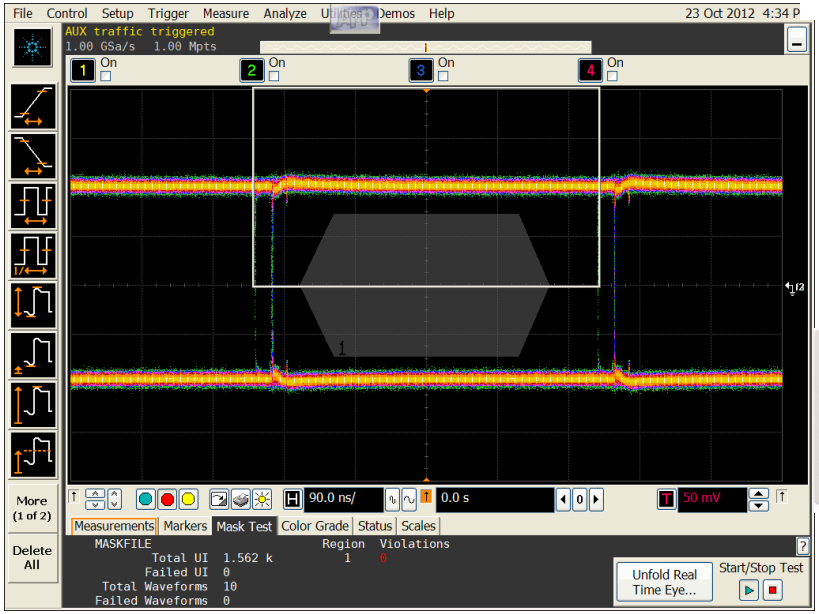


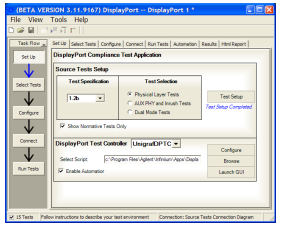
Eye after Equalizer (TP3Eq)

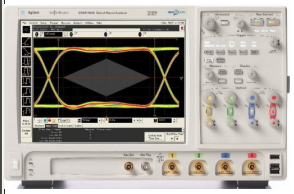
AUX Channel Testing



AUX Eye Testing





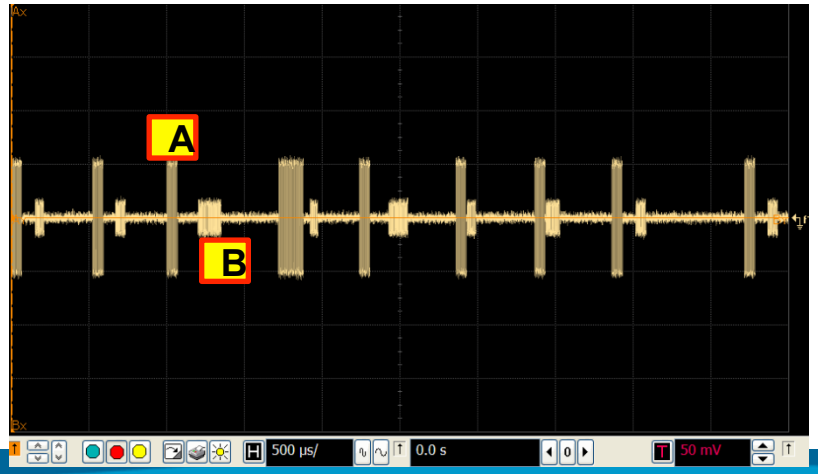


A Source Initiation of AUX communication

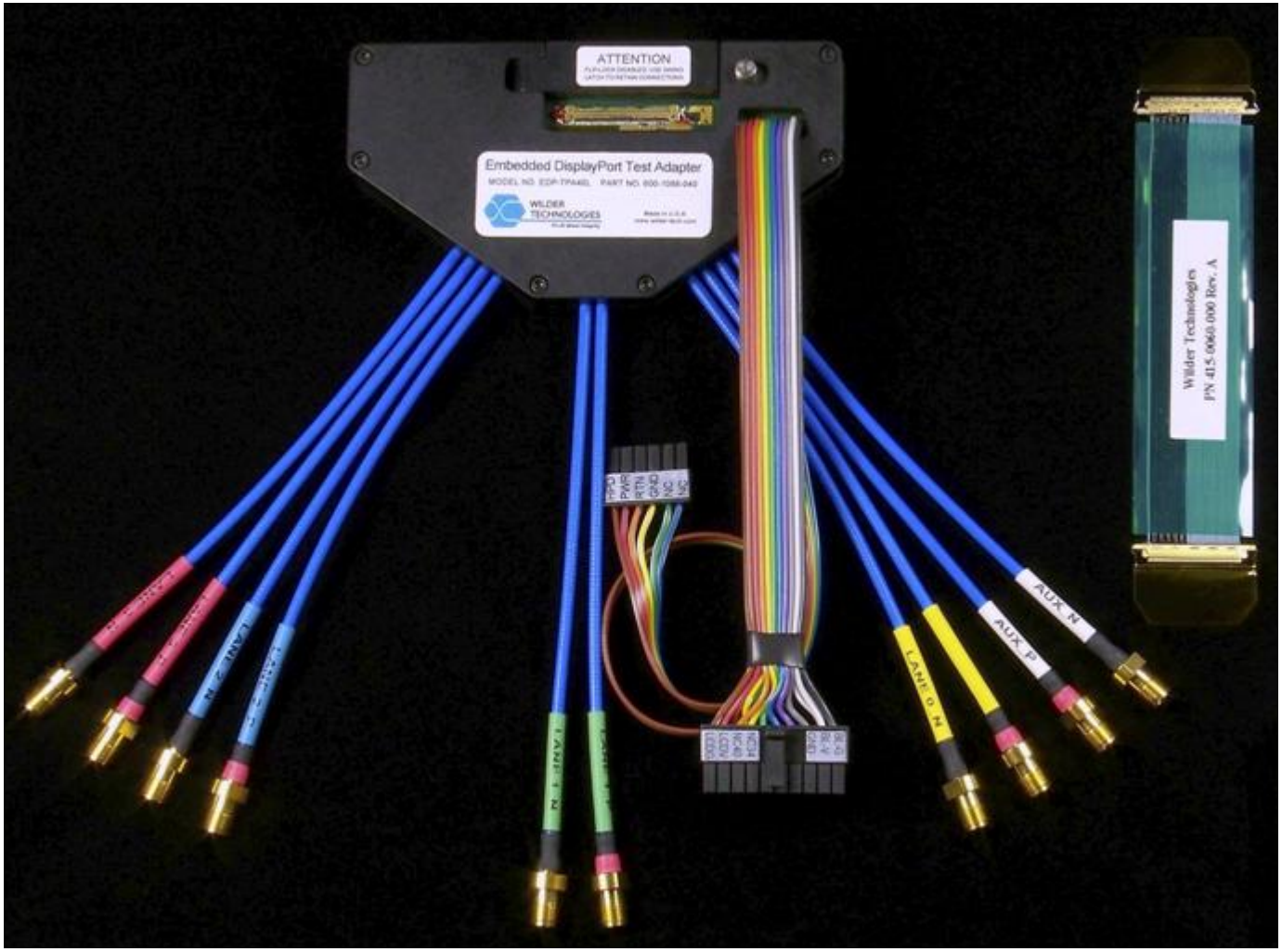
B Receiver Response to Source AUX

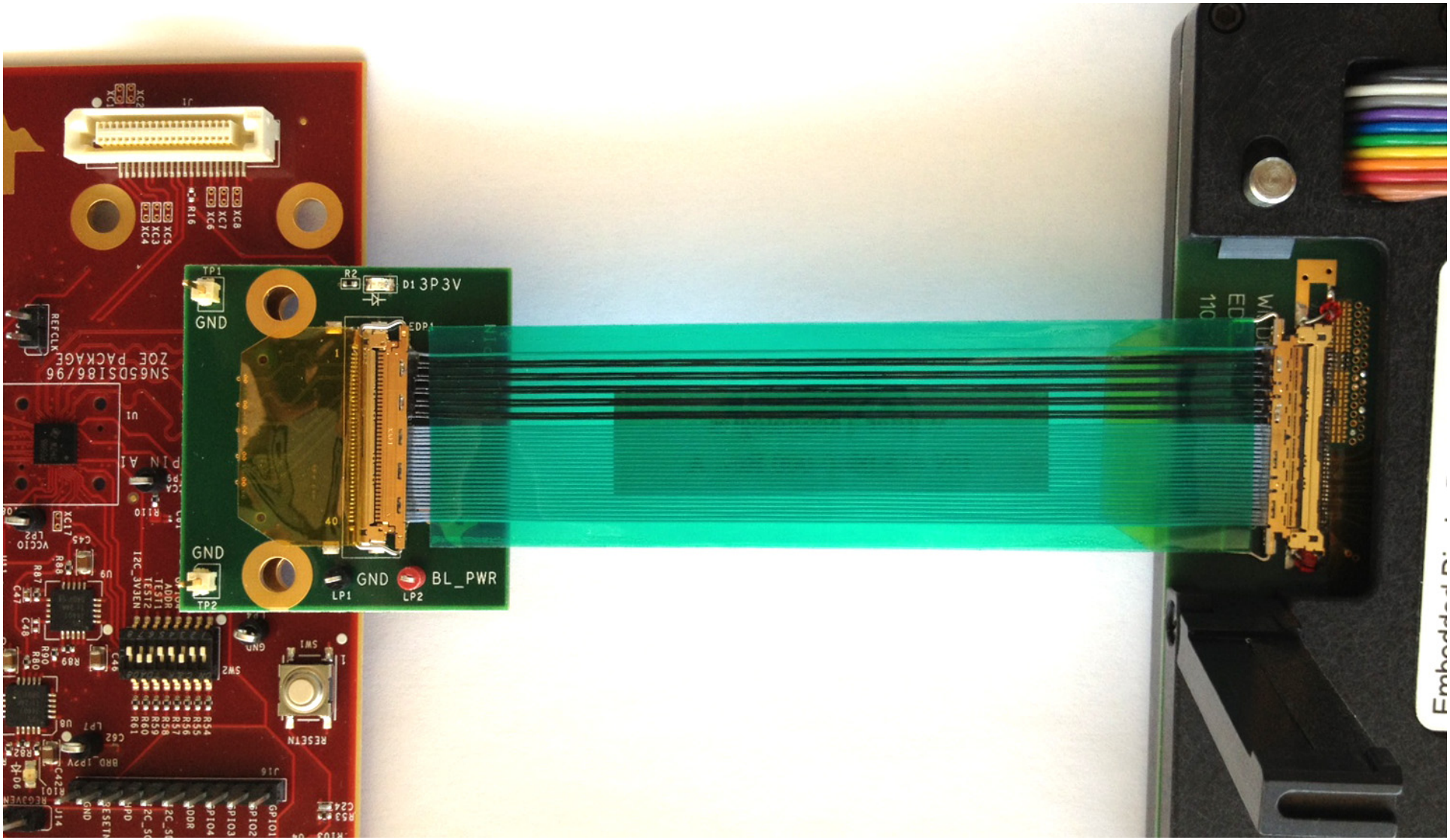
AUX Sensitivity

Reduce the Rx device's AUX level. (100mV shown, 240 spec'd)



eDP1.4 Fixturing




GND
3P3V
GND
GND
BL_PWR
LP1
LP2
TP1
TP2
R2
D1
EDP1
SW1
SW2
RESETN
PIN A1

Testing eDP

A couple of points to make:

1. There is no official compliance program—its embedded so interoperability with other vendors is not a requirement.
2. Use your own connector or pinout→Create your own fixture!
3. Advise to consider validation/verification issues early in process. HPD, Test Mode, level groups.
4. What is tested will be driven by you and your vendor/ customer.

DisplayPort Technology

Continue to expect VESA will continue rolling out value-added capabilities in Display Technologies. Our foundation is solid.

200 members strong-> Industry richness in participation to address the transport and rendering of Display information.

Testing and validation is a core component of our interoperability program and is seen as an ecosystem enabler.