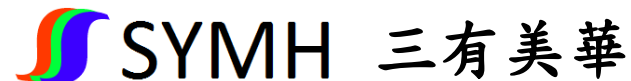




# Tools for DisplayPort™ Testing

Juha Saarinen, Unigraf

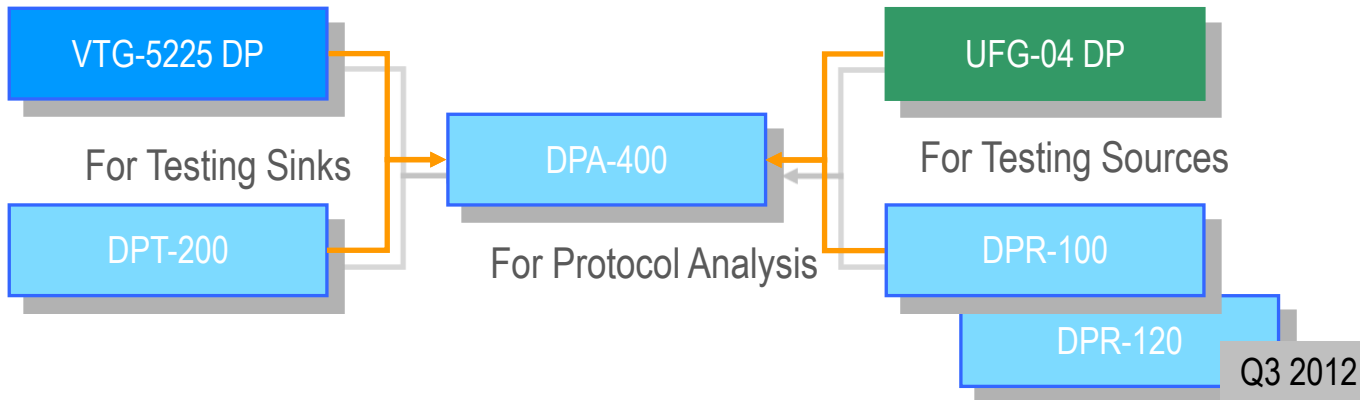
Ping Wang, SYMH Technology Inc  
Unigraf Support Center in Taiwan



# Agenda

- ◆ Unigraf DisplayPort CTS test HW & SW tools
- ◆ LL CTS testing for DisplayPort Sources
- ◆ AUX Channel Monitor
- ◆ LL CTS testing for DisplayPort Sinks
- ◆ Link level debugging tools at RD level
- ◆ Testing at video & audio level
- ◆ Accessories for PHY Testing using Agilent TE
- ◆ Full test automation capabilities

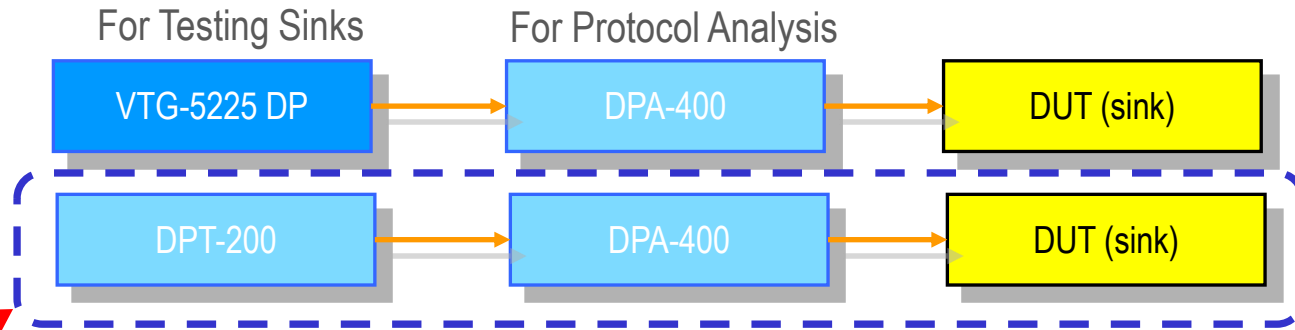
# Unigraf DisplayPort HW set



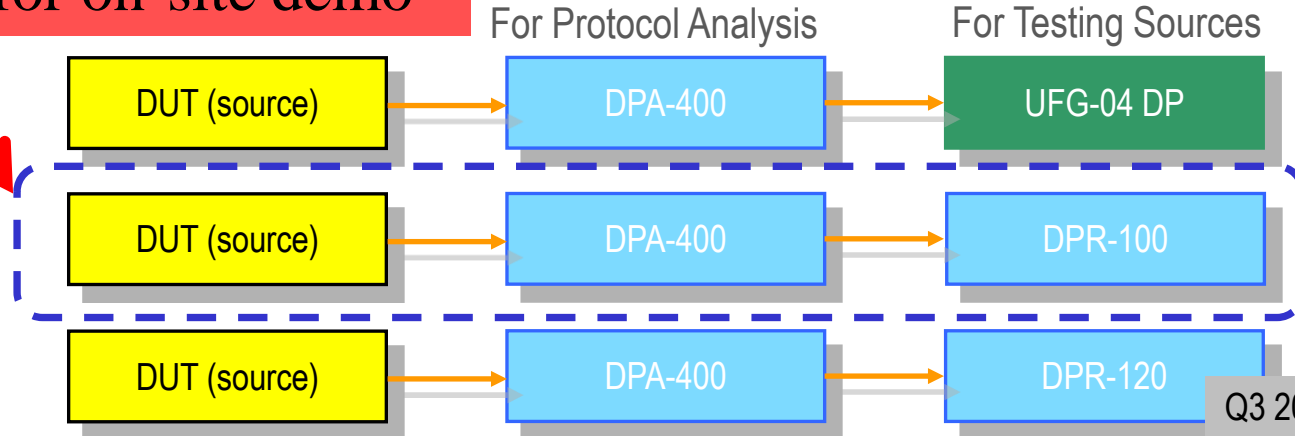
- ◆ VTG-5225 DP: Reference Source w/ full featured PG
- ◆ DPT-200: Compact sized Reference Source
- ◆ UFG-04 DP: Reference Sink w/ full featured grabber
- ◆ DPR-100: Compact sized Reference Sink
- ◆ DPA-400: DP AUX channel monitor



# Unigraf DisplayPort HW set

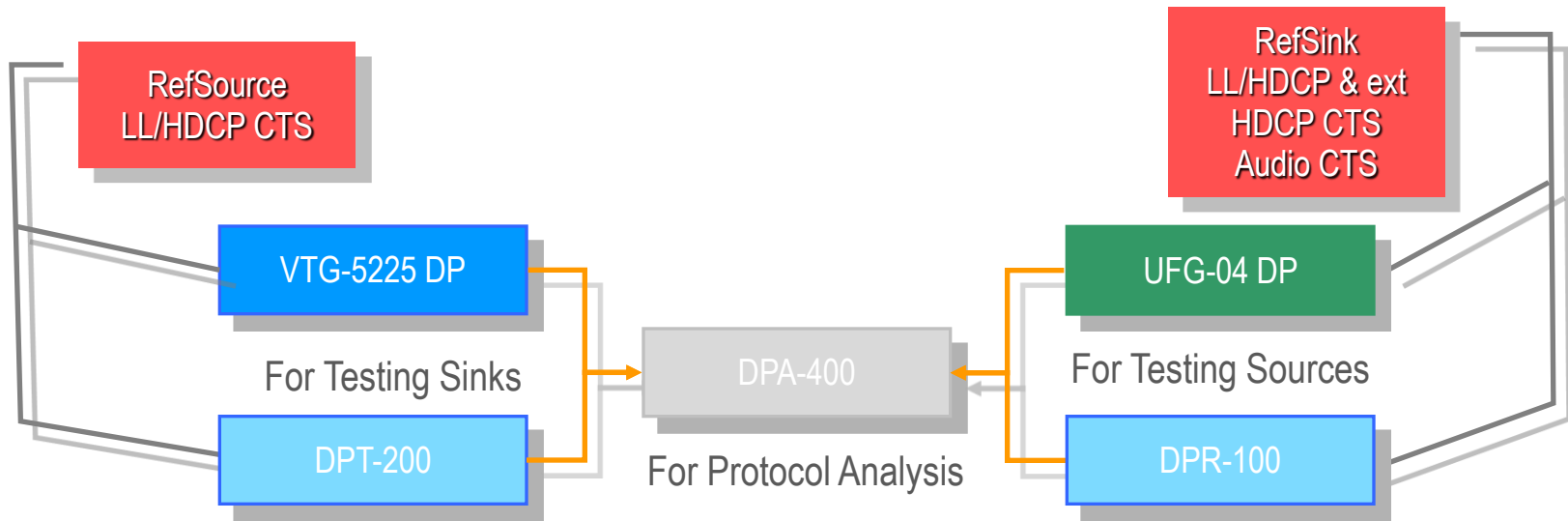


Available for on-site demo



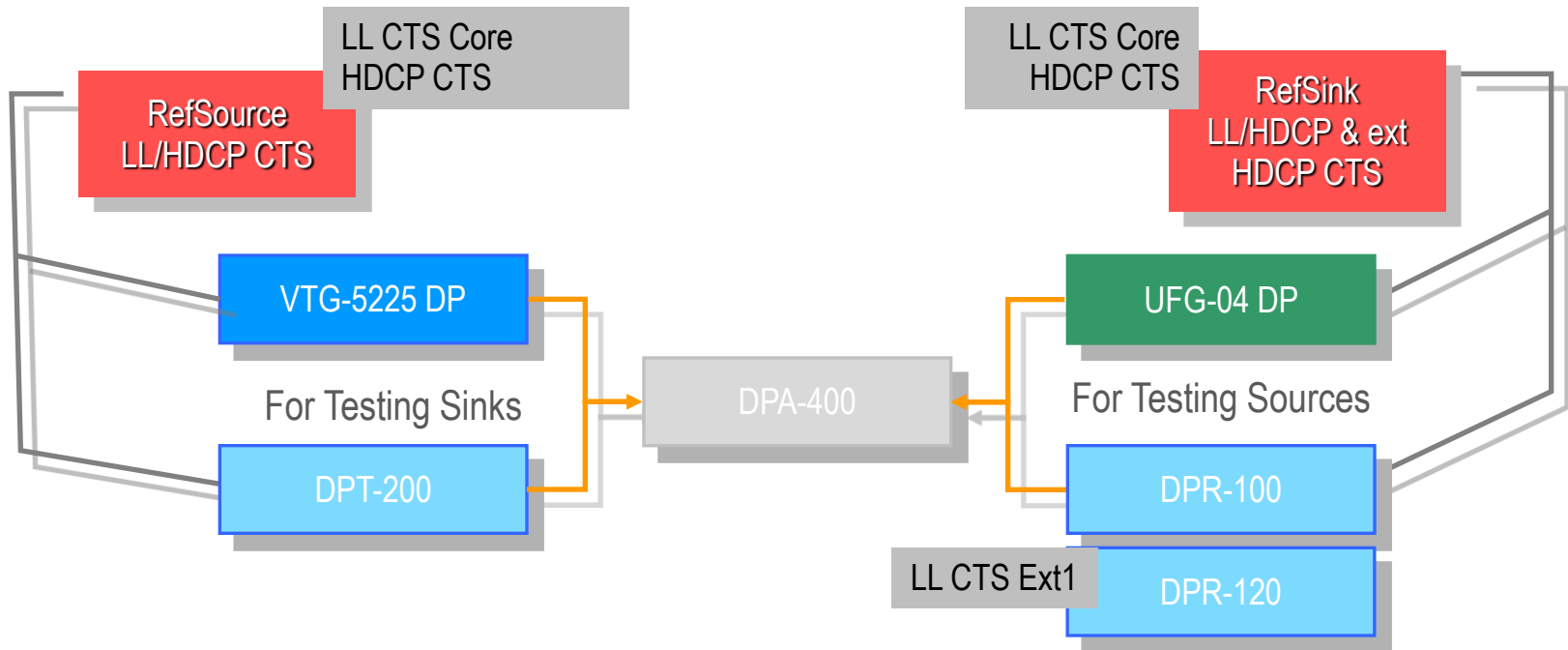
Q3 2012

# Available CTS



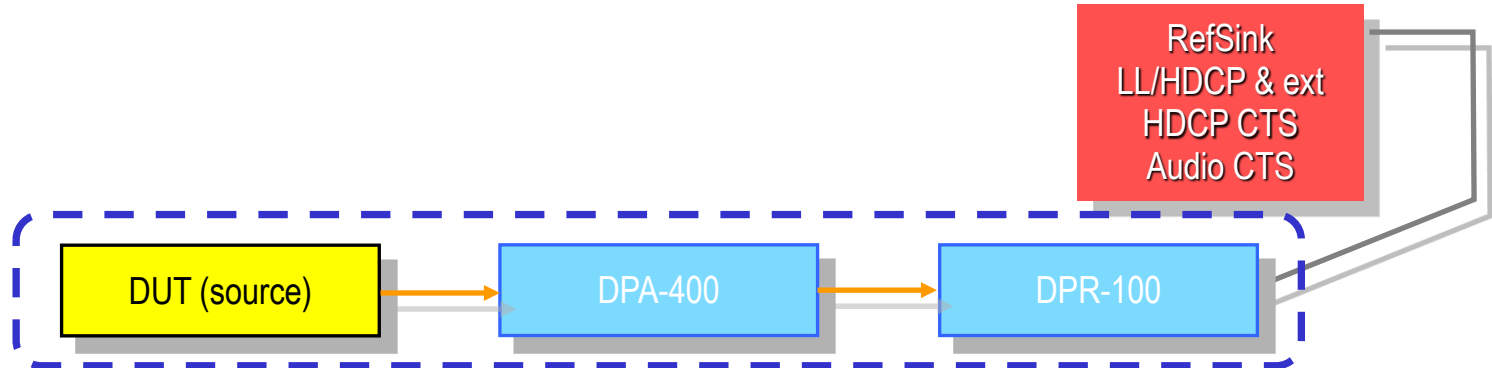
- ◆ RefSource LL / HDCP CTS Tool (VTG-5225 and DPT-200)
- ◆ RefSink LL / HDCP CTS Tool (UFG-04 and DPR-100)
- ◆ RefSink Extended HDCP CTS Tool for repeater devices (UFG-04 and DPR-100)
- ◆ **Certified for ATC (Authorized Test Center)**

# Roadmap for DP 1.2 CTS



- ◆ Existing HW and SW will be used with DP 1.2 LL CTS Core tests
- ◆ Existing HW and SW will be used with DP 1.2 HDCP tests
- ◆ DP 1.2 RefSink CTS Ext 1 available Q4 2012

# Link Layer Testing for DisplayPort Sources



- ◆ A series of tests that check EDID, Link Training, Video and Audio
- ◆ Application is automated, may run all or selected tests
- ◆ Summary and details are in a single report

# Source(DUT) Capabilities

## DUT capabilities

Max lane count: 1 Lane

Max link rate: Low 1.62 Gbps

DUT Capabilities ...

Test Automation ...

Colorimetry support ...

Most packed timings ...

Video Time Stamp Generation ...

Main Link Disable timeout

milliseconds: 2000

TA reset delay (after HPD=0)

milliseconds: 700

TA req. delay (after HPD=1)

milliseconds: 0

Test Runs: 1

Run Tests

Clear Results

Status:

Hide Status

Clear Status

> Licenses available: 'Link Layer Tests', 'HDCP Tests (for Transmitters)', 'HDCP Tests (for Repeaters)', 'Audio Tests'

								Status
5	(4.2.2.3) EDID Read	0	0	0	0	0	0	Idle
6	(4.2.2.4) EDID Read failure #1: I2C-Over-AUX NACK	0	0	0	0	0	0	Idle
7	(4.2.2.5) EDID Read failure #2: I2C-Over-AUX NACK	0	0	0	0	0	0	Idle
8	(4.2.2.6) EDID Read failure #3: I2C-Over-AUX NACK	0	0	0	0	0	0	Idle
9	(4.2.2.7) EDID Read failure #4: I2C-Over-AUX NACK	0	0	0	0	0	0	Idle
10	(4.2.2.8) EDID Read failure #5: I2C-Over-AUX NACK	0	0	0	0	0	0	Idle
11	(4.2.2.9) EDID Read failure #6: I2C-Over-AUX NACK	0	0	0	0	0	0	Idle
12	(4.2.2.10) EDID Read failure #7: I2C-Over-AUX NACK	0	0	0	0	0	0	Idle
13	(4.2.2.11) EDID Read failure #8: I2C-Over-AUX NACK	0	0	0	0	0	0	Idle
14	(4.2.2.12) EDID Read failure #9: I2C-Over-AUX NACK	0	0	0	0	0	0	Idle
15	(4.2.2.13) EDID Read failure #10: I2C-Over-AUX NACK	0	0	0	0	0	0	Idle
16	(4.2.2.14) EDID Read failure #11: I2C-Over-AUX NACK	0	0	0	0	0	0	Idle
17	(4.2.2.15) EDID Read failure #12: I2C-Over-AUX NACK	0	0	0	0	0	0	Idle
18	(4.3.1.7) Successful Link Training at Lower Link Rate due to Loss of...	0	0	0	0	0	0	Idle
19	(4.3.1.8) Unsuccessful Link Training at Lower Link Rate #1: Iterate...	0	0	0	0	0	0	Idle
20	(4.3.1.9) Unsuccessful Link Training at Lower Link Rate #2: Iterate...	0	0	0	0	0	0	Idle
21	(4.3.1.10) Unsuccessful Link Training due to Failure in Channel Equ...	0	0	0	0	0	0	Idle

What you need to know before you start running LL CTS



DUT capabilities

Max lane count: 1 Lane

Max link rate: Low 1.62 Gbps

**DUT Capabilities ...**

Test Automation ...

Colorimetry support ...

Most packed timings ...

Video Time Stamp Generation ...

Main Link Disable timeout  
milliseconds: 2000

TA reset delay (after HPD=0)  
milliseconds: 700

TA req. delay (after HPD=1)  
milliseconds: 0

ID	Test Name	Pass	Fail	Skip	Timeout	Run	Status
1	(4.2.1.1) Source DUT					0	Idle
2	(4.2.1.2) Source Set					0	Idle
3	(4.2.2.1) EDID Read					0	Idle
4	(4.2.2.2) DPCD Rece					0	Idle
5	(4.2.2.3) EDID Read					0	Idle
6	(4.2.2.4) EDID Read					0	Idle
7	(4.2.2.5) EDID Read					0	Idle
8	(4.2.2.6) EDID Corru					0	Idle
9	(4.2.2.7) Branch Dev					0	Idle
10	(4.2.2.8) EDID read					0	Idle
11	(4.2.2.9) E-DDC Fou					0	Idle
12	(4.3.1.1) Successful					0	Idle
13	(4.3.1.2) Successful					0	Idle
14	(4.3.1.3) Successful					0	Idle
15	(4.3.1.4) Successful					0	Idle
16	(4.3.1.5) Successful					0	Idle
17	(4.3.1.6) Successful					0	Idle
18	(4.3.1.7) Successful					0	Idle
19	(4.3.1.8) Unsuccessf					0	Idle
20	(4.3.1.9) Unsuccessf					0	Idle
21	(4.3.1.10) Unsuccessf					0	Idle

DUT Capabilities

Video format change without LT

Lane count reduction without LT

E-DDC

Drive level 3 (1.2V)

Pre-emphasis level 3 (9.5dB)

Fixed Timing

SSC

SSC enabled if MAX\_DOWNSPREAD=1

Accept

Test Runs: 1

Run Tests

Clear Results

Status:

Hide Status

Clear Status

> Licenses available: 'Link Layer Tests', 'HDCP Tests (for Transmitters)', 'HDCP Tests (for Repeaters)', 'Audio Tests'

DUT capabilities

Max lane count: 1 Lane

Max link rate: Low 1.62 Gbps

DUT Capabilities ...

**Test Automation ...**

Colorimetry support ...

Most packed timings ...

Video Time Stamp Generation ...

Main Link Disable timeout  
milliseconds: 2000

TA reset delay (after HPD=0)  
milliseconds: 700

TA req. delay (after HPD=1)  
milliseconds: 0

ID	Test Name	Pass	Fail	Skip	Timeout	Run	Status
1	(4.2.1.1) Source Di		X	0	0	0	Idle
2	(4.2.1.2) Source Re			0	0	0	Idle
3	(4.2.2.1) EDID Rea			0	0	0	Idle
4	(4.2.2.2) DPCD Re			0	0	0	Idle
5	(4.2.2.3) EDID Rea			0	0	0	Idle
6	(4.2.2.4) EDID Rea			0	0	0	Idle
7	(4.2.2.5) EDID Rea			0	0	0	Idle
8	(4.2.2.6) EDID Con			0	0	0	Idle
9	(4.2.2.7) Branch D			0	0	0	Idle
10	(4.2.2.8) EDID rear			0	0	0	Idle
11	(4.2.2.9) E-DDC Fo			0	0	0	Idle
12	(4.3.1.1) Successf			0	0	0	Idle
13	(4.3.1.2) Successf			0	0	0	Idle
14	(4.3.1.3) Successf			0	0	0	Idle
15	(4.3.1.4) Successf			0	0	0	Idle
16	(4.3.1.5) Successf			0	0	0	Idle
17	(4.3.1.6) Successf			0	0	0	Idle
18	(4.3.1.7) Successf			0	0	0	Idle
19	(4.3.1.8) Unsucces			0	0	0	Idle
20	(4.3.1.9) Unsucces			0	0	0	Idle
21	(4.3.1.10) Unsucces			0	0	0	Idle

Test automation

Test Automation support

- TEST\_LINK\_TRAINING
- TEST\_VIDEO\_PATTERN
- TEST\_AUDIO\_PATTERN
- TEST\_TIMING
- TEST\_EDID\_READ

Event indicating DUT ready:

Active Video

Cancel Accept

Test Runs: 1

Run Tests

Clear Results

Status:

Hide Status

Clear Status

> Licenses available: 'Link Layer Tests', 'HDCP Tests (for Transmitters)', 'HDCP Tests (for Repeaters)', 'Audio Tests'

DUT capabilities

Max lane count: 1 Lane

Max link rate: Low 1.62 Gbps

DUT Capabilities ...

Test Automation ...

**Colorimetry support ...**

Most packed timings ...

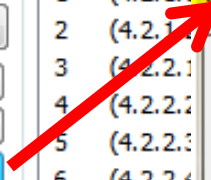
Video Time Stamp Generation ...

Main Link Disable timeout  
milliseconds: 2000

TA reset delay (after HPD=0)  
milliseconds: 700

TA req. delay (after HPD=1)  
milliseconds: 0

ID	Test Name	Pass	Fail	Skip	Timeout	Run	Status
1	(4.2.1.1) Colorimetry						X
2	(4.2.1.2)						
3	(4.2.2.1)						
4	(4.2.2.2)						
5	(4.2.2.3)						
6	(4.2.2.4)						
7	(4.2.2.5)						
8	(4.2.2.6)						
9	(4.2.2.7)						
10	(4.2.2.8)						
11	(4.2.2.9)						
12	(4.3.1.1)						
13	(4.3.1.2)						
14	(4.3.1.3)						
15	(4.3.1.4)						
16	(4.3.1.5)						
17	(4.3.1.6)						
18	(4.3.1.7)						
19	(4.3.1.8)						
20	(4.3.1.9)						
21	(4.3.1.10)						



Format	Bit Depth	Dynamic Range	Color Coeff.
<input checked="" type="checkbox"/> RGB	6	VESA	-
<input checked="" type="checkbox"/> RGB	8	VESA	-
<input type="checkbox"/> RGB	10	VESA	-
<input type="checkbox"/> RGB	8	CEA	-
<input type="checkbox"/> RGB	10	CEA	-
<input type="checkbox"/> YCbCr422	8	CEA	ITU.601
<input type="checkbox"/> YCbCr422	10	CEA	ITU.601
<input type="checkbox"/> YCbCr422	8	CEA	ITU.709
<input type="checkbox"/> YCbCr422	10	CEA	ITU.709
<input type="checkbox"/> YCbCr444	8	CEA	ITU.601
<input type="checkbox"/> YCbCr444	10	CEA	ITU.601
<input type="checkbox"/> YCbCr444	8	CEA	ITU.709
<input type="checkbox"/> YCbCr444	10	CEA	ITU.709

Test Runs: 1

Run Test

Status:

> Licenses available: 'Link Layer Tests', 'HDCP Tests (for

Cancel

Accept

DUT capabilities

Max lane count: 1 Lane

Max link rate: Low 1.62 Gbps

DUT Capabilities ...

Test Automation ...

Colorimetry support ...

**Most packed timings ...**

Video Time Stamp Generation ...

Main Link Disable timeout  
milliseconds: 2000

TA reset delay (after HPD=0)  
milliseconds: 700

TA req. delay (after HPD=1)  
milliseconds: 0

ID	Test Name	Pass	Fail	Skip	Timeout	Run	Status
1	Most Packed timing modes selection						X
2	Most packed timing for 1 lane:						
3	(4)						
4	(4)						
5	(4)						
6	(4)						
7	(4)						
8	Most packed timing for 2 lanes:						
9	(4)						
10	(4)						
11	(4)						
12	(4)						
13	(4)						
14	(4)						
15	(4)						
16	(4)						
17	Most packed timing for 4 lanes:						
18	(4)						
19	(4)						
20	(4)						
21	(4)						

Test Runs: 1

Cancel Accept Results

Status: Hide Status Clear Status

> Licenses available: 'Link Layer Tests', 'HDCP Tests (for Transmitters)', 'HDCP Tests (for Repeaters)', 'Audio Tests'

DUT capabilities

Max lane count: 1 Lane

Max link rate: Low 1.62 Gbps

DUT Capabilities ...

Test Automation ...

Colorimetry support ...

Most packed timings ...

**Video Time Stamp Generation ...**

Main Link Disable timeout  
milliseconds: 2000

TA reset delay (after HPD=0)  
milliseconds: 700

TA req. delay (after HPD=1)  
milliseconds: 0

ID	Test Name	Pass	Fail	Skip	Timeout	Run	Status
1	(4.2.1.1) Source DUT Retry on No-Reply During Aux Read after Ho...	0	0	0	0	0	Idle
2	(4.2.1.2) Source Retry on Invalid Reply During Aux Read after Hot...	0	0	0	0	0	Idle
3	(4.2.2.1) EDID Read upon Hot Plug Event	0	0	0	0	0	Idle
4	(4.2.2.2) DPCD Receiver Capability Read upon Hot Plug Event	0	0	0	0	0	Idle
5	(4.2.2.3) EDID Read	0	0	0	0	0	Idle
6	(4.2.2.4) EDID Read failure #1: I2C-Over-AUX NACK	0	0	0	0	0	Idle
7	(4.2.2.5) EDID Read failure #2: I2C-Over-AUX DEFER	0	0	0	0	0	Idle
8	(4.2.2.6) EDID Corruption Detection	0	0	0	0	0	Idle
9	(4.2.2.7) Branch Device Detection upon HPD Plug Event	0	0	0	0	0	Idle
10	(4.2.2.8) EDID read on IRQ_HPDP event after Branch Device detect...	0	0	0	0	0	Idle
11	(4.2.2.9) E-DDC Four Block EDID Read	0	0	0	0	0	Idle
12	(4.3.1.1) Successful Link Training Upon HPD Plug Event	0	0	0	0	0	Idle
13	(4.3.1.2) Successful Link Training at All Supported Lane Counts an...	0	0	0	0	0	Idle
14	(4.3.1.3) Successful Link Training with Request of Higher Differenti...	0	0	0	0	0	Idle
15	(4.3.1.4) Successful Link Training to a Lower Link Rate #1: Iterate ...	0	0	0	0	0	Idle
16	(4.3.1.5) Successful Link Training to a Lower Link Rate #2: Iterate ...	0	0	0	0	0	Idle



**Video Time Stamp Generation**

	640x480 60 Hz, 18 bpp 25.175 MHz	848x480 60 Hz, 24 bpp 33.750 MHz	1280x720 60 Hz, 24 bpp 74.250 MHz	1280x960 60 Hz, 24 bpp 108.000MHz	1920x1080 60 Hz, 24 bpp 148.500 MHz	1920x1440 60 Hz, 24 bpp 234.000 MHz	None
RBR 1 Lane	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
RBR 2 Lanes	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
RBR 4 Lanes	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>
HBR 1 Lane	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
HBR 2 Lanes	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>
HBR 4 Lanes	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input type="radio"/>	<input checked="" type="radio"/>	<input type="radio"/>

Accept

Test Runs: 1

Status:

> Licenses available: 'Link La

Results

Status

DUT capabilities

Max lane count: 1 Lane

Max link rate: Low 1.62 Gbps

DUT Capabilities ...

Test Automation ...

Colorimetry support ...

Most packed timings ...

Video Time Stamp Generation ...

Main Link Disable timeout  
milliseconds: 2000

TA reset delay (after HPD=0)  
milliseconds: 700

TA req. delay (after HPD=1)  
milliseconds: 0

ID	Test Name	Pass	Fail	Skip	Timeout	Run	Status
1	(4.2.1.1) Source DUT Retry on No-Reply During Aux Read after Ho...	0	0	0	0	0	Idle
2	(4.2.1.2) Source DUT Retry on No-Reply During Aux Read after Ho...	0	0	0	0	0	Idle
3	(4.2.2.1) Source Receiver Capability Read upon Hot Plug Event	0	0	0	0	0	Idle
4	(4.2.2.2) Source Receiver Capability Read upon Hot Plug Event	0	0	0	0	0	Idle
5	(4.2.2.3) EDID Read	0	0	0	0	0	Idle
6	(4.2.2.4) EDID Read failure #1: I2C-Over-AUX NACK	0	0	0	0	0	Idle
7	(4.2.2.5) EDID Read failure #2: I2C-Over-AUX NACK	0	0	0	0	0	Idle
8	(4.2.2.6) EDID Corruption Detection	0	0	0	0	0	Idle
9	(4.2.2.7) Branch Device Detection upon Hot Plug Event	0	0	0	0	0	Idle
10	(4.2.2.8) E-DDC Read on IRQ_HPDS event after Hot Plug	0	0	0	0	0	Idle
11	(4.2.2.9) E-DDC Four Block EDID Read	0	0	0	0	0	Idle
12	(4.3.1.1) Successful Link Training Upon HPD Plug Event	0	0	0	0	0	Idle
13	(4.3.1.2) Successful Link Training at All Supported Lane Counts an...	0	0	0	0	0	Idle
14	(4.3.1.3) Successful Link Training with Request of Higher Differenti...	0	0	0	0	0	Idle
15	(4.3.1.4) Successful Link Training to a Lower Link Rate #1: Iterate ...	0	0	0	0	0	Idle
16	(4.3.1.5) Successful Link Training to a Lower Link Rate #2: Iterate ...	0	0	0	0	0	Idle
17	(4.3.1.6) Successful Link Training with Request of a Higher Pre-em...	0	0	0	0	0	Idle
18	(4.3.1.7) Successful Link Training at Lower Link Rate due to Loss of...	0	0	0	0	0	Idle
19	(4.3.1.8) Unsuccessful Link Training at Lower Link Rate #1: Iterate...	0	0	0	0	0	Idle
20	(4.3.1.9) Unsuccessful Link Training at Lower Link Rate #2: Iterate...	0	0	0	0	0	Idle
21	(4.3.1.10) Unsuccessful Link Training due to Failure in Channel Equ...	0	0	0	0	0	Idle

Some NB needs more time

Controls how long HPD remains low

Test Runs: 1

Run Tests

Clear Results

Status:

Hide Status

Clear Status

> Licenses available: 'Link Layer Tests', 'HDCP Tests (for Transmitters)', 'HDCP Tests (for Repeaters)', 'Audio Tests'

DUT capabilities

Max lane count: 1 Lane

Max link rate: Low 1.62 Gbps

DUT Capabilities ...

Test Automation ...

Colorimetry support ...

Most packed timings ...

Video Time Stamp Generation ...

Main Link Disable timeout

milliseconds: 2000

TA reset delay (after HPD=0)

milliseconds: 700

TA req. delay (after HPD=1)

milliseconds: 0

ID	Test Name	Pass	Fail	Skip	Timeout	Run	Statu
1	(4.2.1.1) Source DUT Retry on No-Reply During Aux Read after Hot Pl...	0	0	0	0	0	Idle
2	(4.2.1.2) Source Retry on Invalid Reply During Aux Read after Hot Plu...	0	0	0	0	0	Idle
3	(4.2.2.1) EDID Read upon Hot Plug Event	0	0	0	0	0	Idle
4	(4.2.2.2) DPCD Receiver Capability Read upon Hot Plug Event	0	0	0	0	0	Idle
5	(4.2.2.3) EDID Read	0	0	0	0	0	Idle
6	(4.2.2.4) EDID Read failure #1: I2C-Over-AUX NACK	0	0	0	0	0	Idle
7	(4.2.2.5) EDID Read failure #2: I2C-Over-AUX DEFER	0	0	0	0	0	Idle
8	(4.2.2.6) EDID Corruption Detection	0	0	0	0	0	Idle
9	(4.2.2.7) Branch Device Detection upon HPD Plug Event	0	0	0	0	0	Idle
10	(4.2.2.8) EDID read on IRQ_HPDP event after Branch Device detection	0	0	0	0	0	Idle
11	(4.2.2.9) E-DDC Four Block EDID Read	0	0	0	0	0	Idle
12	(4.3.1.1) Successful Link Training upon HPD Plug Event	0	0	0	0	0	Idle
13	(4.3.1.2) Successful Link Training at A	0	0	0	0	0	Idle
14	(4.3.1.3) Successful Link Training with	0	0	0	0	0	Idle
15	(4.3.1.4) Successful Link Training to a Lower Link Rate #1: Iterate at ...	0	0	0	0	0	Idle
16	(4.3.1.5) Successful Link Training to a Lower Link Rate #2: Iterate at ...	0	0	0	0	0	Idle
17	(4.3.1.6) Successful Link Training with Request of a Higher Pre-empha...	0	0	0	0	0	Idle
18	(4.3.1.7) Successful Link Training at Lower Link Rate due to Loss of Sv...	0	0	0	0	0	Idle
19	(4.3.1.8) Unsuccessful Link Training	0	0	0	0	0	Idle
20	(4.3.1.9) Unsuccessful Link Training	0	0	0	0	0	Idle

Select tests

Run Tests

Test Runs: 1

Run Tests

Clear Results

Status:

Hide Status

Clear Status

> Licenses available: 'Link Layer Tests', 'HDCP Tests (for Transmitters)', 'HDCP Tests (for Repeaters)', 'Audio Tests'

Number of runs

DUT capabilities

Max lane count: 1 Lane

Max link rate: Low 1.62 Gbps

DUT Capabilities ...

Test Automation ...

Colorimetry support ...

Most packed timings ...

Video Time Stamp Generation ...

Main Link Disable timeout  
milliseconds: 2000

TA reset delay (after ...  
milliseconds: 700

TA req. delay (after HPD=1)  
milliseconds: 0

ID	Test Name	Pass	Fail	Skip	Timeout	Run	Status
1	(4.2.1.1) Source DUT Retry on No-Reply During Aux Read after Hot Pl...	1	0	0	0	1	Idle
2	(4.2.1.2) Source Retry on Invalid Reply During Aux Read after Hot Plu...	1	0	0	0	1	Idle
3	(4.2.2.1) EDID Read upon Hot Plug Event	1	0	0	0	1	Idle
4	(4.2.2.2) DPCD Receiver Capability Read upon Hot Plug Event	0	1	0	0	1	Idle
5	(4.2.2.3) EDID Read	0	1	0	0	1	Idle
6	(4.2.2.4) EDID Read failure #1: I2C-Over-AUX NACK	1	0	0	0	1	Idle
7	(4.2.2.5) EDID Read failure #2: I2C-Over-AUX DEFER	0	0	0	0	0	Run
8	(4.2.2.6) EDID Corruption Detection	0	0	0	0	0	Idle
9	(4.2.2.7) Branch Device Detection upon HPD Plug Event	0	0	0	0	0	Idle
10	(4.2.2.8) EDID read on IRQ_HPDP event after Branch Device detection	0	0	0	0	0	Idle
11	(4.2.2.9) E-DDC Four Block EDID Read	0	0	0	0	0	Idle
12	(4.2.2.10) EDID Read failure #3: I2C-Over-AUX NACK	0	0	0	0	0	Idle
13	(4.2.2.11) EDID Read failure #4: I2C-Over-AUX DEFER	0	0	0	0	0	Idle
14	(4.3.1.3) Successful Link Training with Request of Higher Differential V...	0	0	0	0	0	Idle
15	(4.3.1.4) Successful Link Training to a Lower Link Rate #1: Iterate at ...	0	0	0	0	0	Idle
16	(4.3.1.5) Successful Link Training to a Lower Link Rate #2: Iterate at ...	0	0	0	0	0	Idle
17	(4.3.1.6) Successful Link Training with Request of a Higher Pre-empha...	0	0	0	0	0	Idle
18	(4.3.1.7) Successful Link Training at Lower Link Rate due to Loss of Sy...	0	0	0	0	0	Idle
19	(4.3.1.8) Unsuccessful Link Training at Lower Link Rate #1: Iterate at ...	0	0	0	0	0	Idle
20	(4.3.1.9) Unsuccessful Link Training at Lower Link Rate #2: Iterate at ...	0	0	0	0	0	Idle

Status update while running tests

Test Runs: [input field]

Abort

Clear Results

Status:

Hide Status

Clear Status

Received video timing is 1024 X 768  
WARNING: resolution is not 640x480  
Test 6 PASSED.

Running test 7 ...



DUT capabilities

Max lane count: 1 Lane

Max link rate: Low 1.62 Gbps

DUT Capabilities ...

Test Automation ...

Colorimetry support ...

Most packed timings ...

Video Time Stamp Generation

milliseconds: 700

TA req. delay (after HPD=1) milliseconds: 0

ID	Test
1	(4)
2	(4)
3	(4)
4	(4)
5	(4)
6	(4)
7	(4)
8	(4)
9	(4)
10	(4)
11	(4)
12	(4)
13	(4)
14	(4)
15	(4)
16	(4)
17	(4)

Additional Data for Report

DP Source DUT	DP Reference Sink TE
Device Name: dut001	Model: abc
Model: A-1	Serial Number: 123
Serial Number: 789	Driver Revision: 1.1
Driver Revision: 3.2	

Additional Comments

Report created using the Unigraf DisplayPort Reference Sink Software 1.1.81



Save to File: C:\Users\user\Desktop\dut001 LL CTS.HTM

Save Report Cancel

File --> save report

Test Runs: 1

Status: Clear Results Clear Status

Test 10 FAILED, step 8, substep 0: Timeout elapsed.

Running test 11 ...

Test 11 SKIPPED: DUT does not support E-DDC protocol

# DisplayPort Source Compliance Test Report

Click item to see details

## CONTENTS

- Test Summary
- General Information
- View all test details

### View details by test

- 1 - (4.2.1.1) Source DUT Retry
- 2 - (4.2.1.2) Source Retry on Invalid Reply
- 3 - (4.2.2.1) EDID Read upon Hot Plug Event
- 4 - (4.2.2.2) DPCD Receiver Capability Read upon Hot Plug Event
- 5 - (4.2.2.3) EDID Read
- 6 - (4.2.2.4) EDID Read failure #1: I2C-Over-AUX NACK
- 7 - (4.2.2.5) EDID Read failure #2: I2C-Over-AUX DEFER
- 8 - (4.2.2.6) EDID Corruption Detection
- 9 - (4.2.2.7) Branch Device Detection upon HPD Plug Event
- 10 - (4.2.2.8) EDID read on IRQ\_HP
- 10 - (4.2.2.8) EDID read on IRQ\_HP event after Branch Device detection
- 11 - (4.2.2.9) E-DDC Four Block EDID Read

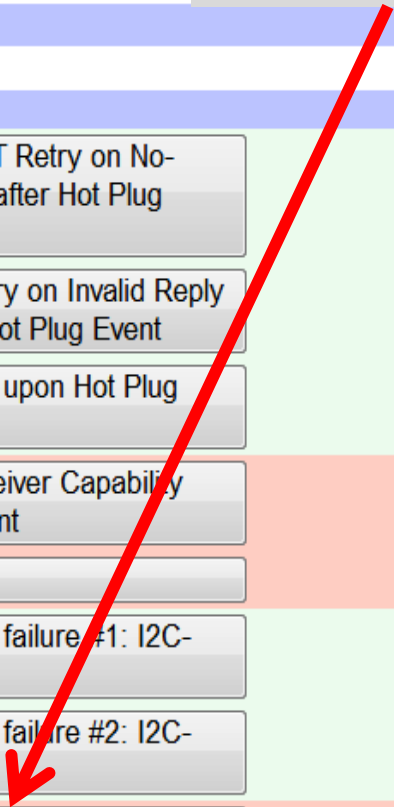
Printer Friendly

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## TEST SUMMARY

TEST	PASSED	FAILED	TIMED OUT	SKIPPED
1 - (4.2.1.1) Source DUT Retry on No-Reply During Aux Read after Hot Plug Event	1	0	0	0
2 - (4.2.1.2) Source Retry on Invalid Reply During Aux Read after Hot Plug Event	1	0	0	0
3 - (4.2.2.1) EDID Read upon Hot Plug Event	1	0	0	0
4 - (4.2.2.2) DPCD Receiver Capability Read upon Hot Plug Event	0	1	0	0
5 - (4.2.2.3) EDID Read	0	1	0	0
6 - (4.2.2.4) EDID Read failure #1: I2C-Over-AUX NACK	1	0	0	0
7 - (4.2.2.5) EDID Read failure #2: I2C-Over-AUX DEFER	1	0	0	0
8 - (4.2.2.6) EDID Corruption Detection	0	1	0	0
9 - (4.2.2.7) Branch Device Detection upon HPD Plug Event	1	0	0	0
10 - (4.2.2.8) EDID read on IRQ_HP event after Branch Device detection	0	1	0	0
11 - (4.2.2.9) E-DDC Four Block EDID Read	0	0	0	1



## TEST DETAILS

### 8 - (4.2.2.6) EDID Corruption Detection

PASSED 0

FAILED 1

TIMED OUT 0

SKIPPED 0

Test 8; "8 - (4.2.2.6) EDID Corruption Detection" - Run 1  
Started 2012-04-28, 14:15:55

Max lane count: 1 Lane, Max link rate: Low 1.62 Gbps  
TEST\_LINK\_TRAINING: Yes, TEST\_VIDEO\_PATTERN: Yes, TEST\_TIMING: Yes, TEST\_EDID\_READ: Yes  
TEST\_AUDIO\_PATTERN: Yes, Event indicating DUT ready: Active Video  
Video format change without re-training: No, Lane count reduction without re-training: No,  
E-DDC: No, Drive level 3 (1.2V): No, Pre-emphasis level 3 (9.5dB) No,  
Fixed Timing No, Spread Spectrum: No, SSC enabled (if MAX\_DOWNSPREAD=1): No  
Main link disable timeout: 2000ms, TA reset delay (after HPD=0): 700ms, TA req. delay (after HPD=1): 0ms

-----  
De-asserting HPD  
Setting TEST\_EDID\_READ=1  
Asserting HPD  
Setting 5 s timeout  
Waiting for EDID read request  
128 byte EDID read detected  
Setting 5 s timeout  
Waiting for active video with fail-safe timing  
Active video detected  
Received video timing is 1024 X 768  
Test FAILED, step 7, substep 0: Resolution is not 640x480.

DUT  
conditions

Testing steps  
& results

Check Link CTS manual.

Search for 4.2.2.6

Result: The device fails if the Source DUT does not read the entire EDID block through AUX CH before transmission of the main video stream, test timeout or interrupt by test operator. It also fails if the Source DUT does not transmit the main video using the fail-safe mode.

## TEST DETAILS

### 11 - (4.2.2.9) E-DDC Four Block EDID Read

PASSED 0

FAILED 0

TIMED OUT 0

SKIPPED 1

Test 11; "11 - (4.2.2.9) E-DDC Four Block EDID Read" - Run 1

Started 2012-04-28, 14:16.09

Max lane count: 1 Lane, Max link rate: Low 1.62 Gbps

TEST\_LINK\_TRAINING: Yes, TEST\_VIDEO\_PATTERN: Yes, TEST\_TIMING: Yes, TEST\_EDID\_READ: Yes

TEST\_AUDIO\_PATTERN: Yes, Event indicating DUT ready: Active Video

Video format change without re-training: No, Lane count reduction without re-training: No,

E-DDC: No, Drive level 3 (1.2V): No, Pre-emphasis level 3 (9.5dB) No,

Fixed Timing No, Spread Spectrum: No, SSC enabled (if MAX\_DOWNSPREAD=1): No

Main link disable timeout: 2000ms, TA reset delay (after HPD=0): 700ms, TA req. delay (after HPD=1): 0ms

Test SKIPPED: DUT does not support E-DDC protocol

File Tools Help

Link Layer Tests **HDCP Tests (for Transmitters)** HDCP Tests (for Repeaters) Audio Tests Link Training E-EDID

DUT capabilities

- CP\_IRQ used for R0' read
- CP\_IRQ used for READY read
- Output when DEVICE\_COUNT=0
- Encryption enable bootstrapping

Authentication start timeout  
seconds: 10.0

HDCP Authentication status

ID	Test Name	Pass	Fail	Skip	Timeout	Run	Status
1	(1A-01) Regular Procedure: With Receiver	0	0	0	0	0	Idle
2	(1A-02) Regular Procedure: HPD After Writing Aksv	0	0	0	0	0	Idle
3	(1A-03) Regular Procedure: HPD During Link Integrity Check Stage	0	0	0	0	0	Idle
4	(1A-04) Irregular Procedure: (First Part of Authentication) Failure t...	0	0	0	0	0	Idle
5	(1A-05) Irregular Procedure: (First Part of Authentication) Verify B...	0	0	0	0	0	Idle
6	(1A-06) Irregular Procedure: (First Part of Authentication) Verify R0?	0	0	0	0	0	Idle
7	(1A-07) Irregular Procedure: (Link Integrity Check) Link Integrity F...	0	0	0	0	0	Idle
8	(1A-08) Irregular Procedure: SRM	0	0	0	0	0	Idle
9	(1A-09) Regular Procedure: Encryption Disable Bootstrapping	0	0	0	0	0	Idle
10	(1B-01) Regular Procedure: With Repeater	0	0	0	0	0	Idle
11	(1B-02) Irregular Procedure: Spurious CP_IRQ Interrupt	0	0	0	0	0	Idle
12	(1B-03) Regular Procedure: HPD After Reading R0'	0	0	0	0	0	Idle
13	(1B-04) Irregular Procedure: (Second part of Authentication) Time...	0	0	0	0	0	Idle
14	(1B-05) Irregular Procedure: (Second part of Authentication) Verify V'	0	0	0	0	0	Idle
15	(1B-06) Irregular Procedure: (Second part of Authentication) MAX_...	0	0	0	0	0	Idle
16	(1B-07) Irregular Procedure: (Second part of Authentication) MAX_...	0	0	0	0	0	Idle

Test Runs: 1

Run Tests

Clear Results

Status:

Hide Status

Clear Status

> Licenses available: 'Link Layer Tests', 'HDCP Tests (for Transmitters)', 'HDCP Tests (for Repeaters)', 'Audio Tests'



File Tools Help

Link Layer Tests HDCP Tests (for Transmitters) HDCP Tests (for Repeaters) Audio Tests Link Training **E-EDID**

## E-EDID Encoder / Decoder

## Collection 1

... Blocks in collection

## Block 0 [VESA EDID]

... Checksum

## Version

... Extension flag

▷ Vendor &amp; Product ID

▷ Basic Display Parameters and F

▷ Display x,y Chromacity coordin.

▷ Established timings I and II

▷ Manufacturer's Timings

▷ Standard Timings

▷ 18-Byte data blocks

## Block 1 [CEA 861]

... Checksum

## CEA Extensions Version

... Sink Underscans IT video

... Basic audio

... YCbCr (4:4:4)

... YCbCr (4:2:2)

... Native DTD's in entire E-EDID

Details of "":

Key	Value
Unigraf E-EDID Codec	V1.0.20
Blocks in collection	2



Load



Save



Show Hex



Show Log



Write EDID



Read EDID

Status:

▼ Hide Status

Clear Status

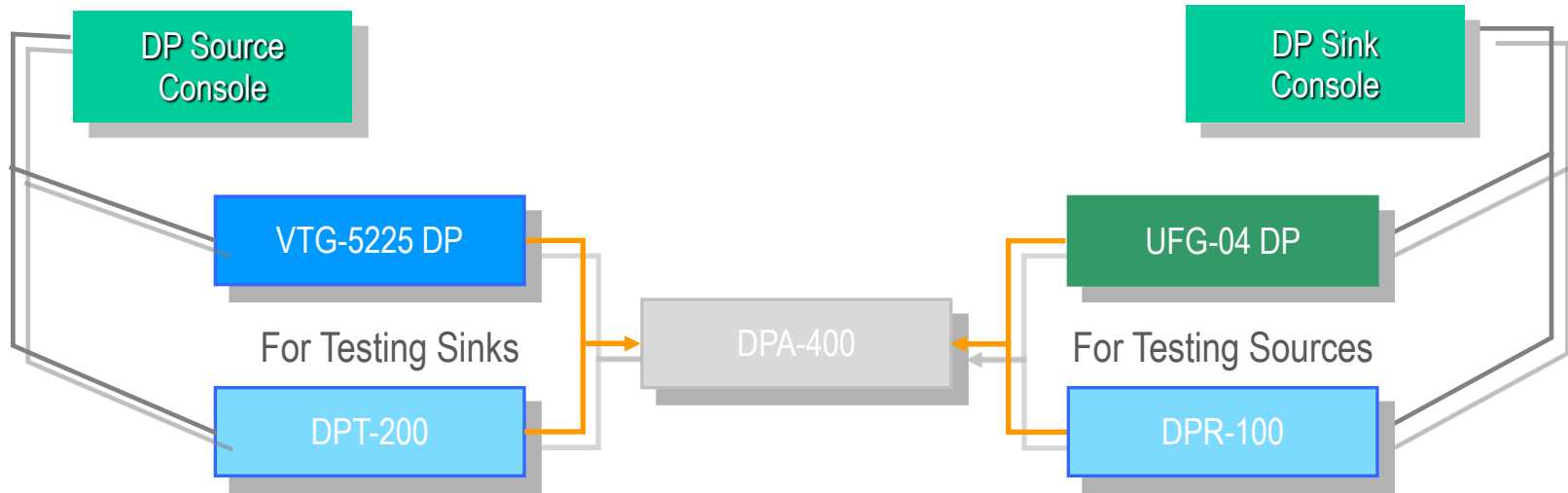
```
> Read E-EDID Block #0
> Read E-EDID Block #0 -1
> Read E-EDID Block #1
```

Tools → options

Longer delay between tests may help get more stable measurements

ID	Test Name	Pass	Fail	Skip	Timeout	Run	Status
1	(4.2.1.1) Source DUT Retry on No-Reply During Aux Read after Ho...	0	0	0	0	0	Idle
2	(4.2.1.2) Source Retry on Invalid Reply During Aux Read after Hot...	0	0	0	0	0	Idle
3	(4.2.2.1) EDID Read upon Hot Plug Event	0	0	0	0	0	Idle
4	(4.2.2.2) DPCD Receiver Capability Read upon Hot Plug Event	0	0	0	0	0	Idle
5	(4.2.2.3) EDID Read						Idle
6	(4.2.2.4) EDID Read						Idle
7	(4.2.2.5) EDID Read						Idle
8	(4.2.2.6) EDID Read						Idle
9	(4.2.2.7) EDID Read						Idle
10	(4.2.2.8) EDID Read						Idle
11	(4.2.2.9) E-DDC Four						Idle
12	(4.3.1.1) Successful						Idle
13	(4.3.1.2) Successful						Idle
14	(4.3.1.3) Successful						Idle
15	(4.3.1.4) Successful						Idle
16	(4.3.1.5) Successful						Idle
17	(4.3.1.6) Successful						Idle
18	(4.3.1.7) Successful						Idle
19	(4.3.1.8) Unsuccess						Idle
20	(4.3.1.9) Unsuccess						Idle
21	(4.3.1.10) Unsuccess						Idle

# R&D Link Level Debugging Tools



- ◆ Source and Sink Consoles for Link Level debug
- ◆ Complete status monitoring of the DP interface
- ◆ Allows for manual "tweaking" of the DP link parameters
- ◆ User friendly GUI and computer interface



# Sink Console for helping debug

The screenshot shows the DP Sink Console v1.1.4 - Unigraf interface. The 'Main' tab is active, displaying device connection details, link status, and a table of Main Stream Attributes (MSA).

**Device connection:** Serial port: DPR-100 USB Serial Port (COM), Firmware version: 3.1.0, Update firmware... button.

**Link status:** L0, L1, L2, L3 (all green), Clock recovery, Symbol lock, Channel equalization, Voltage swing (mVpp), Pre-emphasis (dB), Lane count: 4, Bit rate (Gbps): 2.70, Framing mode: Enhanced, Scrambling: Disabled. Error count: 7FFF 7FFF 7FFF 7FFF, Clear button, Update button.

**Video CRC:** Red: N/A, Green: N/A, Blue: N/A, Update button.

**Main Stream Attributes (MSA):** Enable checked, Unstable, Video valid. Copy, Clear buttons.

Time stamp	CLK	FORMAT	RANGE	COLORIMETRY	BPC	MODE	HSTA...	HTOT	HACT	HS POL	HSYNC	VSTART	VTOT	VACT	VS P
22:51:13															
22:51:27															
22:52:09															
22:52:19															
22:52:23	Async	RGB	VESA	ITU-R BT601-5	8	Prog	296	1344	1024	Pos	136	35	806	768	Pos
22:53:07															

**Diagram:** DUT (source) → DPA-400 → DPR-100

**Messages:** Setting AUX channel output level... Command successful. Testing AUX channel sensitivity... Test finished. Copy, Clear buttons.

**Footer:** Firmware version: 3.1.0, DPR-100 USB Serial Port (COM14)

Sink capabilities

**Maximum lane count**

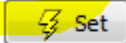
1  2  4

**Maximum link rate (Gbps)**

1.62  2.70

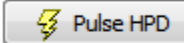
**Framing mode**

Normal  Enhanced



Hot plug detect (HPD) pulse

**Duration (ms)**




AUX channel output level

**Voltage swing (mVpp)**

200  270  400

600  800  1200




AUX Channel Sensitivity Test

**Start value (mVpp)**

**Stop value (mVpp)**

**Decrement (mVpp)**

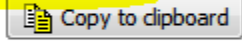
30  50  100




```


Testing 400 mVpp... OK
Testing 300 mVpp... OK
Testing 200 mVpp... OK
Testing 100 mVpp... OK
Testing 50 mVpp... FAILED
Test finished.

```



DPCD access

Source/target address (hex):  

Data (hex):  


Previous action: None


Messages

Setting AUX channel output level...  
Command successful.

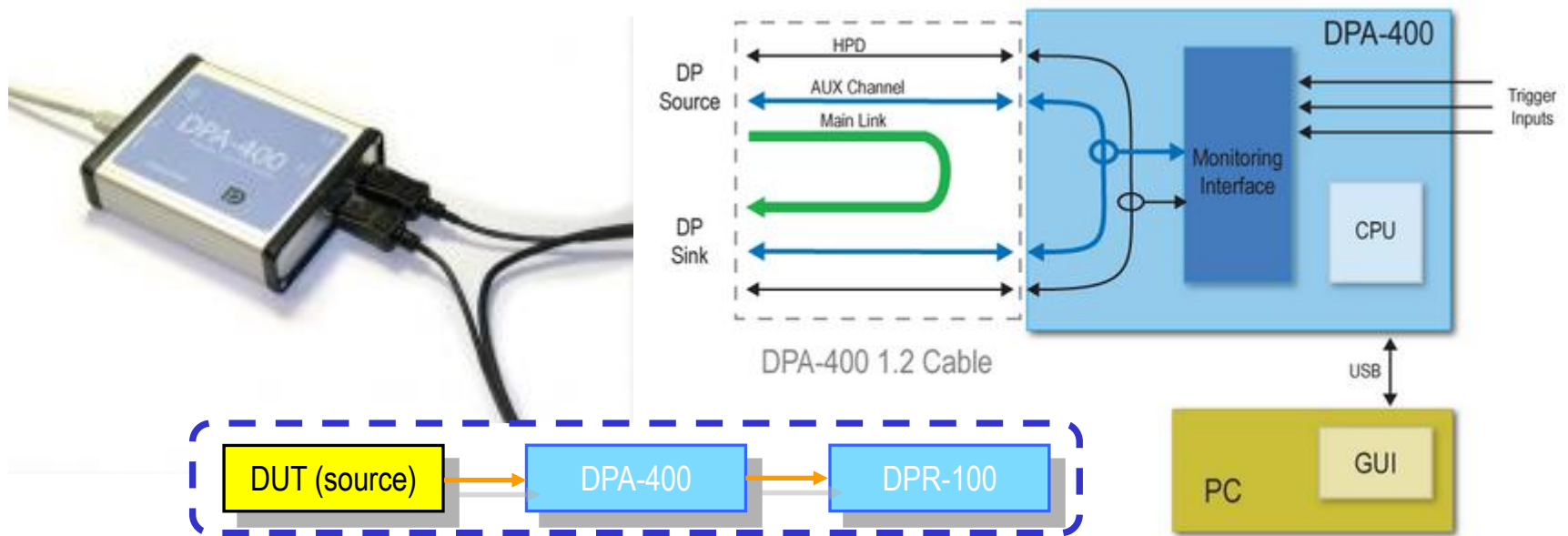
Testing AUX channel sensitivity...  
Test finished.



 Copy

 Clear

# AUX Channel Monitor



- ◆ Full DP AUX channel traffic analysis
- ◆ Each message time stamped, raw data and decoded information available
- ◆ Set trigger points and data filters for evaluating specific events
- ◆ Record and trigger HPD and external inputs

**Aux channel monitor**

File Search Tools Help

Filters

- Show Events
- Show I2C
- Show Native
- Show HDCP

Stop Acquisition

Pause Download

Line	Timestamp	From	Type	Details	Data
60	11398.27	Source	Native	Req WR 4 bytes to 0x00103	80 01 03 03 ...
61	11398.69	Sink	Native	AUX_DEFER, 0 bytes	20
62	11398.72	Source	Native	Req WR 4 bytes to 0x00103	80 01 03 03 ...
63	11399.14	Sink	Native	AUX_DEFER, 0 bytes	20
64	11399.20	Source	Native	Req WR 4 bytes to 0x00103	80 01 03 03 ...
65	11399.58	Sink	Native	AUX_DEFER, 0 bytes	20
66	11399.65	Source	Native	Req WR 4 bytes to 0x00103	80 01 03 03 ...
67	11400.03	Sink	Native	AUX_DEFER, 0 bytes	20
68	11400.10	Source	Native	Req WR 4 bytes to 0x00103	80 01 03 03 ...
69	11400.26	Sink	Native	AUX_ACK, 0 bytes	00
70	11400.32	Source	Native	Req RD 6 bytes from 0x00202	90 02 02 05
71	11400.38	Sink	Native	AUX_ACK, 6 bytes	00 11 11 00 ...
72	11400.48	Source	Native	Req WR 4 bytes to 0x00103	80 01 03 03 ...
73	11400.90	Sink	Native	AUX_DEFER, 0 bytes	20
74	11400.93	Source	Native	Req WR 4 bytes to 0x00103	80 01 03 03 ...
75	11401.34	Sink	Native	AUX_DEFER, 0 bytes	20
76	11401.38	Source	Native	Req WR 4 bytes to 0x00103	80 01 03 03 ...
77	11401.44	Sink	Native	AUX_DEFER, 0 bytes	20
78	11401.48	Source	Native	Req WR 4 bytes to 0x00103	80 01 03 03 ...
79	11401.54	Sink	Native	AUX_ACK, 0 bytes	00
80	11402.08	Source	Native	Req RD 6 bytes from 0x00202	90 02 02 05
81	11402.18	Sink	Native	AUX_ACK, 6 bytes	00
82	11402.27	Source	Native	Req WR 5 bytes to 0x00102	80 01 03 03 ...
83	11402.40	Sink	Native	AUX_ACK, 0 bytes	00
84	11569.57	Source	Native	Req RD 1 bytes from 0x00202	90
85	11569.63	Sink	Native	AUX_ACK, 1 bytes	00
86	11570.37	Source	Native	Req RD 1 bytes from 0x00203	90
87	11570.43	Sink	Native	AUX_ACK, 1 bytes	00
88	11571.20	Source	Native	Req RD 4 bytes from 0x00103	90 01 03 03 ...
89	11571.26	Sink	Native	AUX_ACK, 4 bytes	00
90	11572.03	Source	Native	Req RD 1 bytes from 0x00206	90
91	11572.13	Sink	Native	AUX_ACK, 1 bytes	00
92	11572.83	Source	Native	Req RD 1 bytes from 0x00207	90
93	11572.90	Sink	Native	AUX_ACK, 1 bytes	00

Message details:

Line #93 -

setting adjust)  
0x00207 := 0x88

VOLTAGE\_SWING\_LANE2 = level 0

**Customizable highlights**

**Select events**

Options

Communications

Connect using COM: 10 (@115200 8N1)

Graphics options

Select new font: Current font "Tahoma", size 10

Default font color: [Black]

Default background color: [White]

Selected item font color: [White]

Selected item background color: [Blue]

Highlighted item font color: [White]

Highlighted item background color: [Green]

Colored address ranges:

Rule #0 - RD/WR from 00102 to 00106 Font Color: [White]

Rule #1 - RD/WR from 00202 to 00207 Background Color: [White]

Rule #2 - RD from 00050 to 00050

Add ... Edit ... Remove Up Down

Help Cancel Accept

Status Acquisition running - Downloading data Downloaded 1768 Bytes Buffered 0

# Link Layer Testing for DisplayPort Sinks

The screenshot shows the 'Unigraf Reference Source CTS with HDCP' application window. The 'Link layer tests' tab is selected, displaying a table of tests. The 'DUT capabilities' section on the left has several options highlighted with a yellow circle: 'Fixed Timing', 'More than 1 segment in EDID', 'DUT Colorimetry support ...', and 'Most packet timings...'. The test results table is as follows:

ID	Test Name	Pass	Fail	Skip	Timeout	Run	Status
1	(5.2.1.1) Read One Byte from Valid DPCD Address	0	0	0	0	0	Idle
2	(5.2.1.2) DPCD Receiver Capability Read (Read Twelve By...	0	0	0	0	0	Idle
3	(5.2.1.3) Write One Byte to Valid DPCD Address	0	0	0	0	0	Idle
4	(5.2.1.4) Write Nine Bytes to Valid DPCD Addresses	0	0	0	0	0	Idle
5	(5.2.1.5) Write EDID Offset (One Byte I2C-Over-Aux Write)	0	0	0	0	0	Idle
6	(5.2.1.6) Read One EDID Byte (One Byte I2C-Over-Aux R...	0	0	0	0	0	Idle
7	(5.2.1.7) EDID Read (1 Byte I2C-Over-Aux Segment Writ...	0	0	0	0	0	Idle
8	(5.2.1.8) Illegal Aux Request Syntax	0	0	0	0	0	Idle

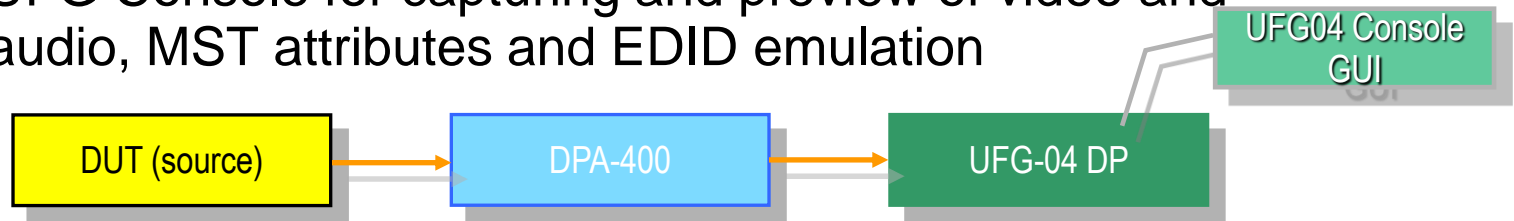
Below the screenshot, a diagram illustrates the testing setup. A red box labeled 'RefSource LL/HDCP CTS' is connected to a blue dashed box containing 'DPT-200' and 'DPA-400'. An orange arrow points from 'DPA-400' to a yellow box labeled 'DUT (sink)'. A green diagonal banner across the diagram reads 'Available for on-site demo'. The email address 'ywang@symmtech.com' is visible in the bottom right corner.

- Equally powerful tools for testing/debugging DP sinks

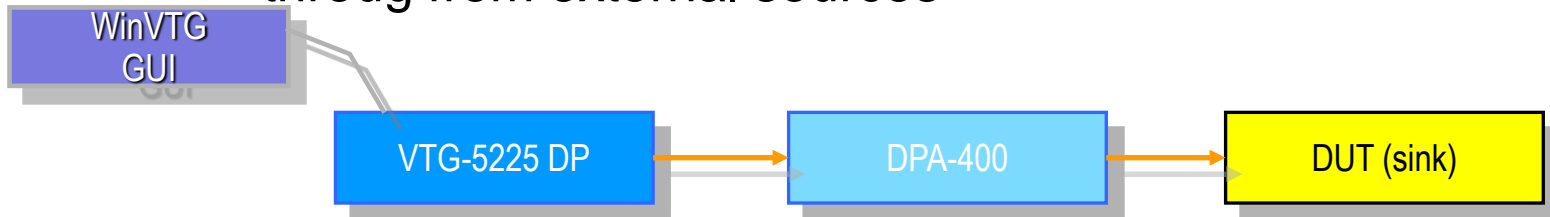
Available for on-site demo

# Testing at Video and Audio Level

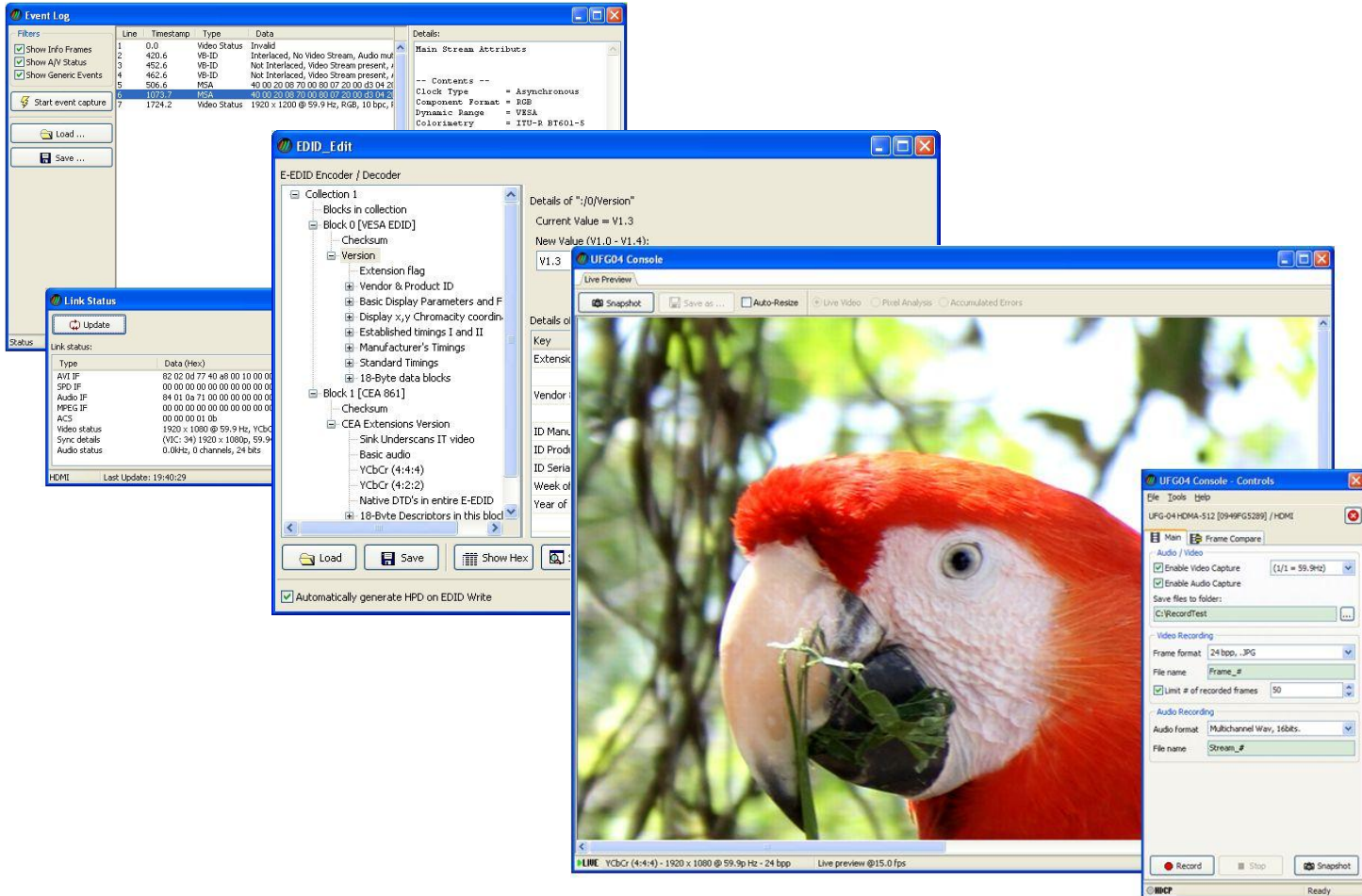
- ◆ UFG Console for capturing and preview of video and audio, MST attributes and EDID emulation



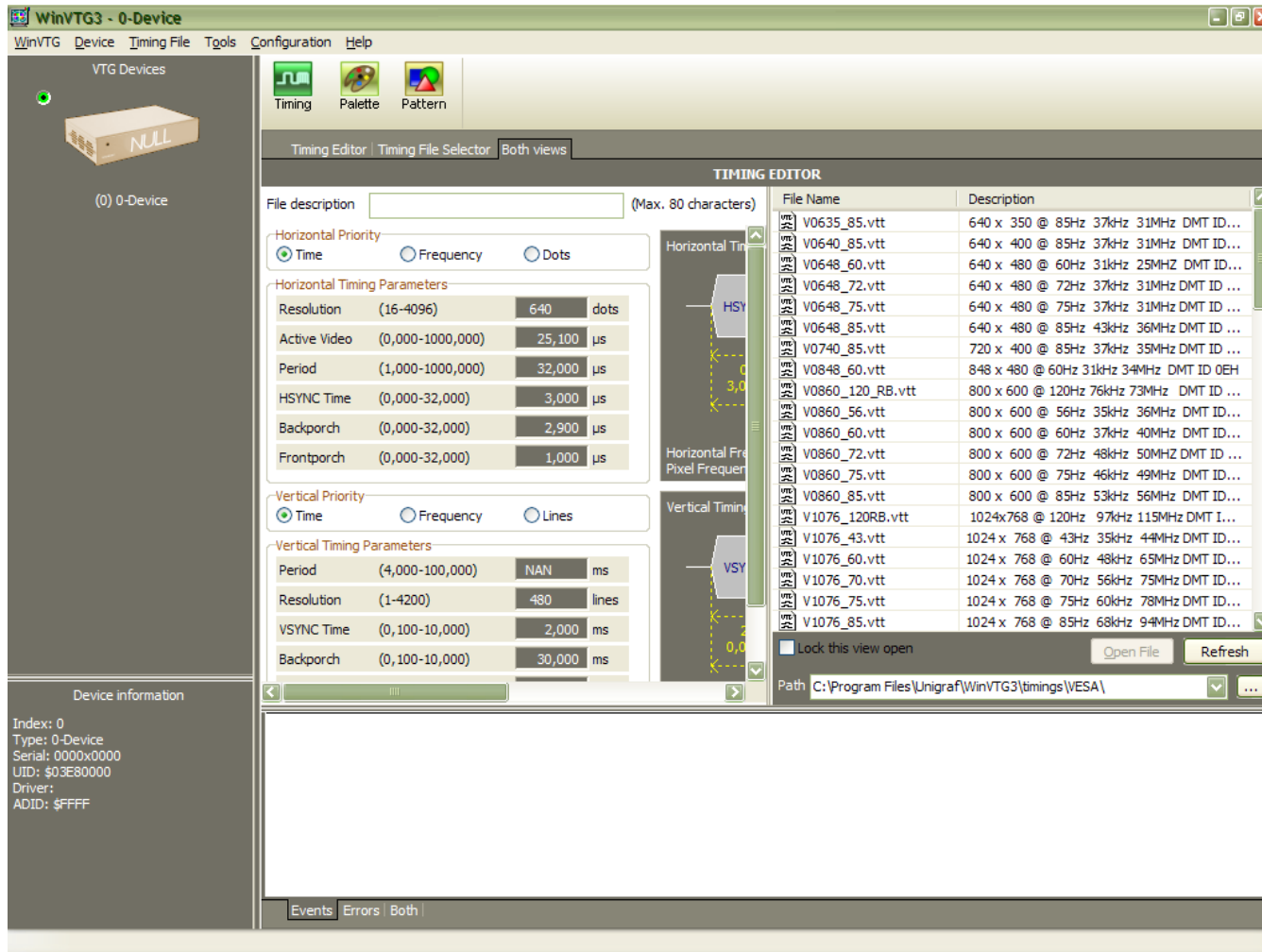
- ◆ WinVTG for full control of the video timing, audio pass through from external sources



# UFG Console

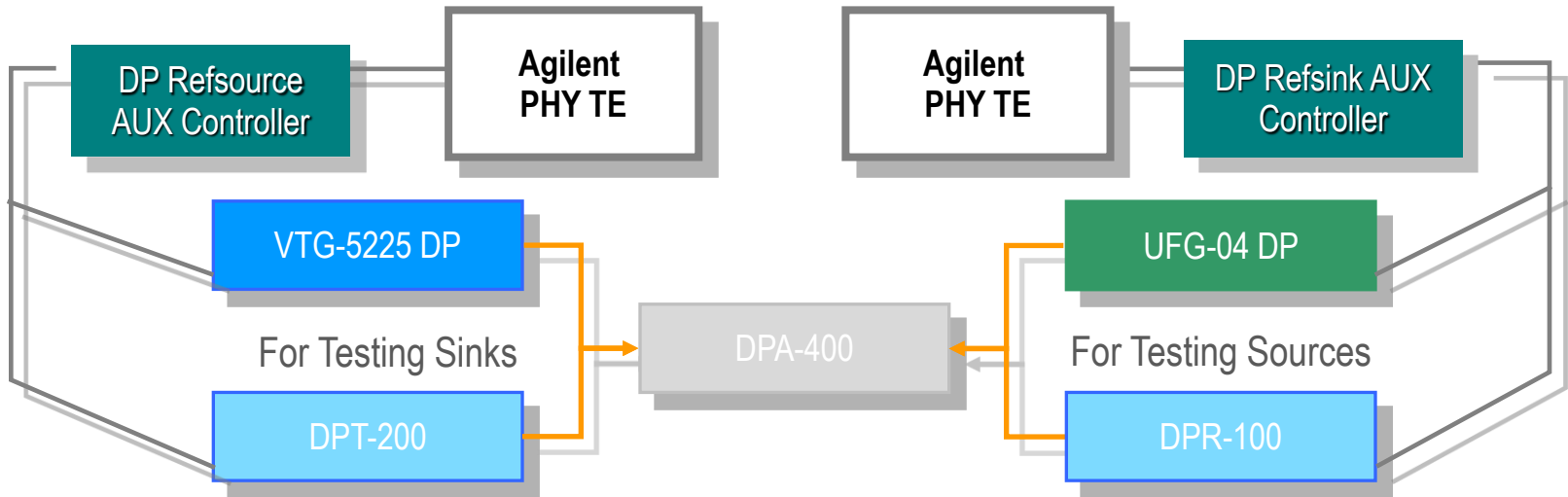


# WinVTG



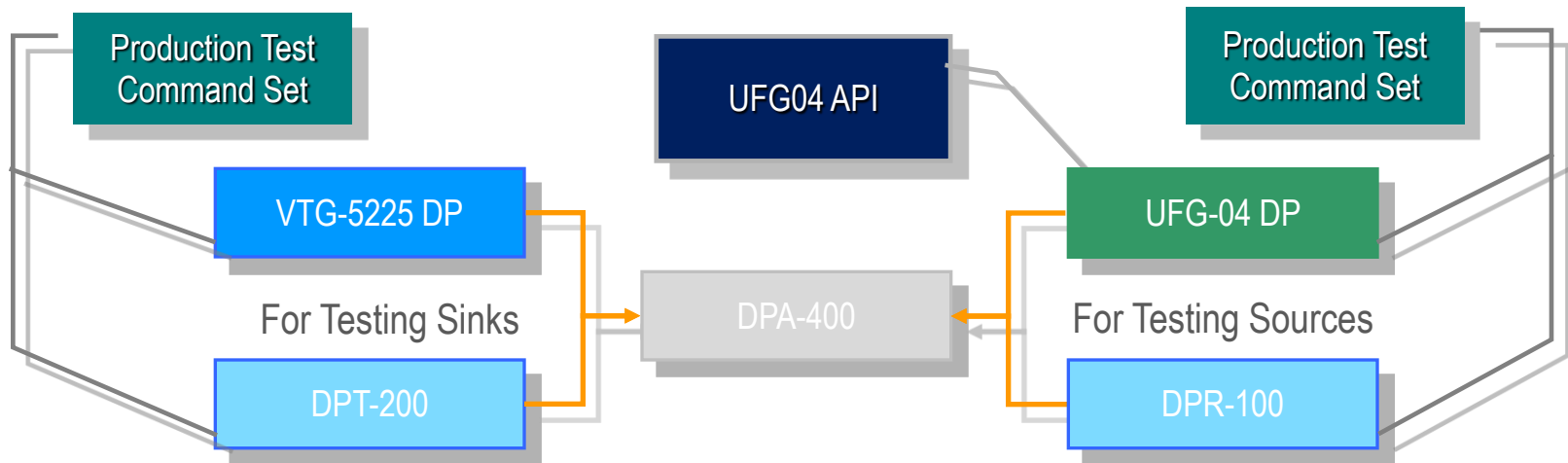


# Accessories for PHY Testing



- ◆ DP RefSource and RefSink provide full compatibility for automated testing with Agilent DSO90000A series oscilloscopes and the J-BERT N4903B using the U7232B and N5990A test automation software packages.
- ◆ Can be used with all Unigraf RefSinks or RefSources

# Full Test Automation Capabilities



- ◆ Production Test Command Set (PTC) for both RefSource and RefSink devices
  - Communication over USB / RS232
- ◆ UFG SDK for UFG-04 DP
  - Application Interface API (DLL)
  - Ready to use application examples for C++, Python, VB

# Summary

- ◆ Unigraf has a full set of HW, CTS tools and AUX Channel monitor
- ◆ DP Console GUI for sinks and sources allows RD debugging at Link Level
- ◆ **Knowing your DUT capabilities and referencing CTS manual can greatly help passing CTS**
- ◆ Unigraf products also enable production test automation to reduce production costs for OEM