DisplayPort 1.2 Receiver Testing

April 2012

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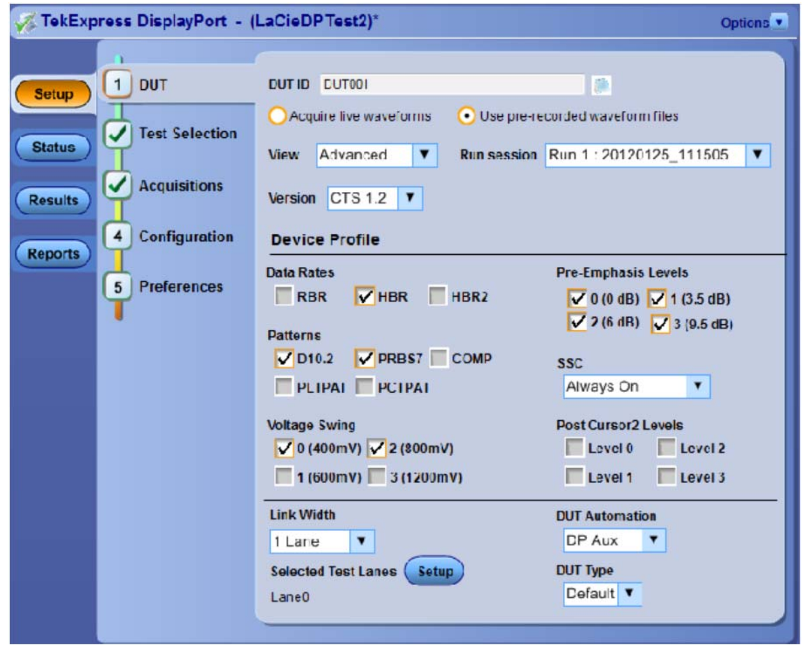
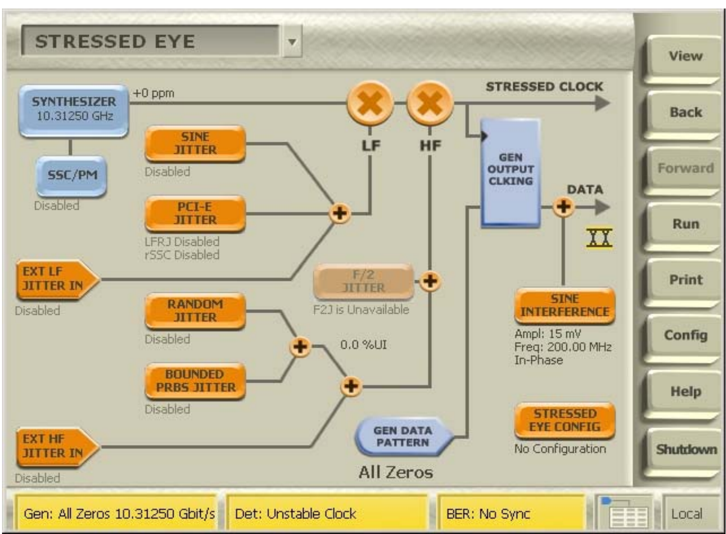
DisplayPort Physical Layer Validation



Automated Transmitter Testing

- Fully automated 17 core DP1.2 Physical Layer TX measurements.
- Comprehensive AUX channel automation through Tektronix DP-AUX interface.
- RF-Switch aware automation permits standalone PVT operation of over 1700 different scope based measurements.



Receiver Testing

- DisplayPort Freq Lock/Symbol Lock/ PRBS7 pattern sequencing
- DP-AUX error counter checks internal error counters through standard DP internal error registers.
- Complete Rx test solution
  - 12.5 GHz BERTScope
  - 12.5 GHz real-time scope
  - ISI board or Active ISI generation for signal impairment
  - DisplayPort plug fixture + DP-AUX controller

Physical Setup → ISI Calibration → RJ calibration → SJ calibration → AC Common Mode calibration → Eye Height Calibration and TJ → RX Testing

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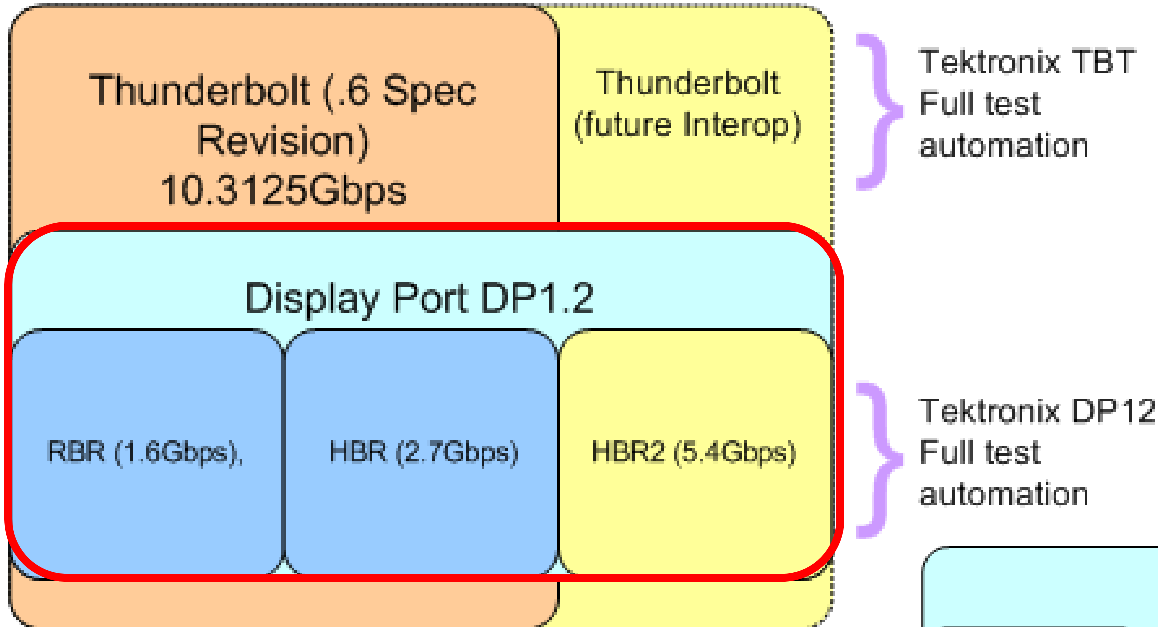
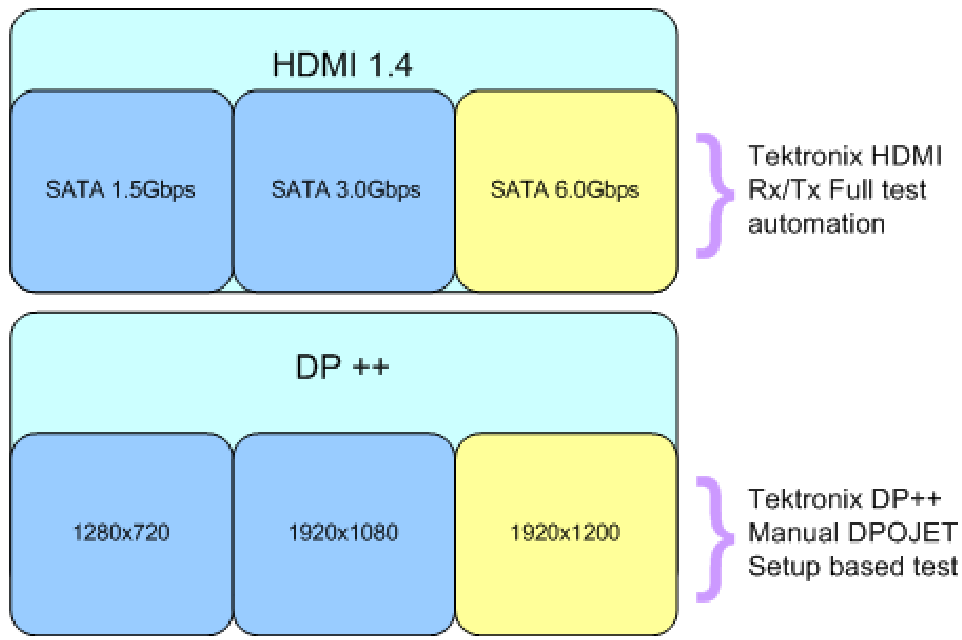
DisplayPort Electrical Validation Ecosystem



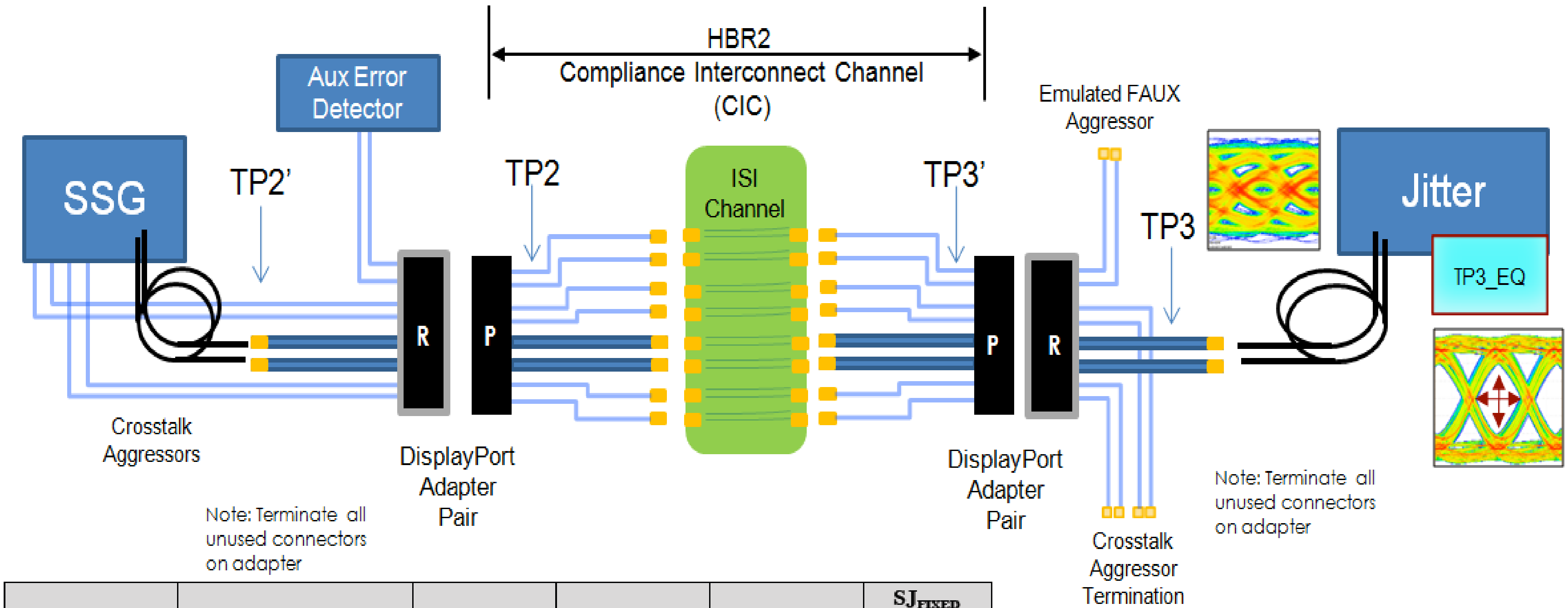


Thunderbolt Receiver test Diversity

- The display technology interface ecosystem demands a multitude of standards be checked both on Tx and Rx.
- Demands broad test expertise to cover both DisplayPort, HDMI and DP++

DisplayPort 1.2
Sink (Rx) Test Overview

Receiver testing is performed with a Tektronix BSA125C BertScope, DP-AUX controller and Tektronix BSA-ISI Channel board. BER observation times range from 37 seconds 10.5 minutes depending on the data rate and jitter frequency being tested. A DSA125C 12.5GHz bandwidth oscilloscope is used not only to Tx test automation but also for Rx signal calubration.



f(SJ)	TJ(JTHBR2rx)	ISI	RJ(RMS)	Approximate SJ_{SWEEP}	SJ_{FIXED} @ 200MHz
[MHz]	[mUI]	[mUI]	[mUI]	[mUI]	[mUI]
2	1026	220	16.7	505	100
10	636	220	16.7	116	100
20	624	220	16.7	104	100
100	620	220	16.7	100	100

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Receiver Test Electrical Conditions

Stressed Eye Parameter		RBR	HBR	HBR2
Transition Time Converter (TTC) Value		150ps	150ps	100ps
Bit Rate		1.6Gb/s	2.7Gb/s	5.4Gb/s
Calibration Test Point		TP3	TP3_Eq	TP3_Eq
Test Signal Pattern		PRBS7	PRBS7	HBR2 CompEye
Compliance Channel (CIC)	ISI	570mUI	161mUI	220mUI
Rj (RMS)		8.1mUI	13.5mUI	16.7mUI
Sj_{FIXED} @ 200MHz		NA	NA	100mUI
Sj_{SWEEP} Approximate 2MHz		981mUI	904mUI	505mui
10MHz		111mUI	225mUI	116mUI
20MHz		80mUI	182mUI	104mUI
100MHz		NA	168mUI	100mU
Calibrated Eye Height +/- 10%		46mV	150mV	90mV
SSC	33 KHz, triangular shaped, 5000 ppm			
Pre-Emphasis		No	No	No
Crosstalk Pattern		D24.3 (quarter rate Clock)		
Crosstalk Amplitude (mV:		134@TP3	700@TP2	700@TP2

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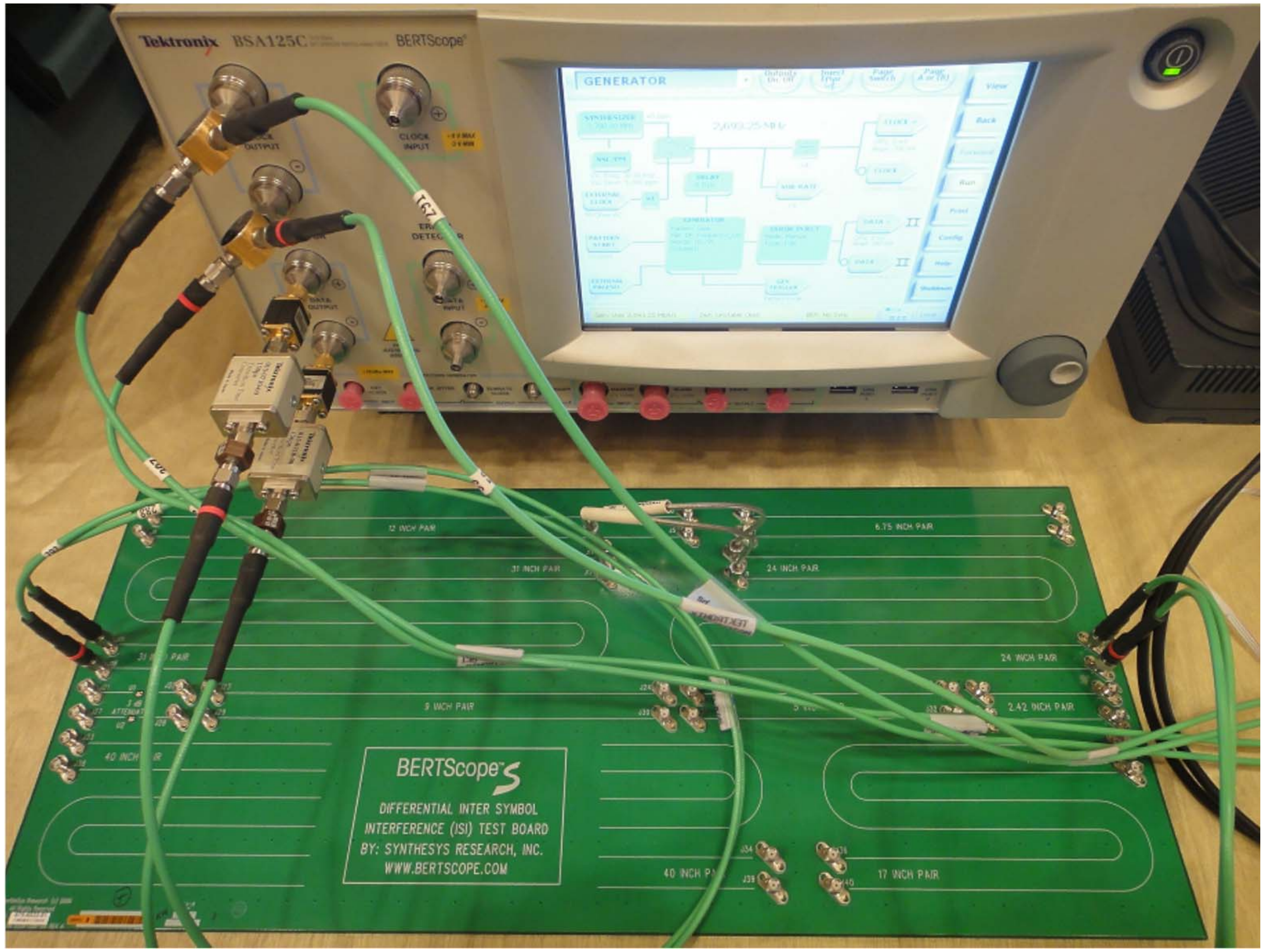
BertScope Receiver Test Solution

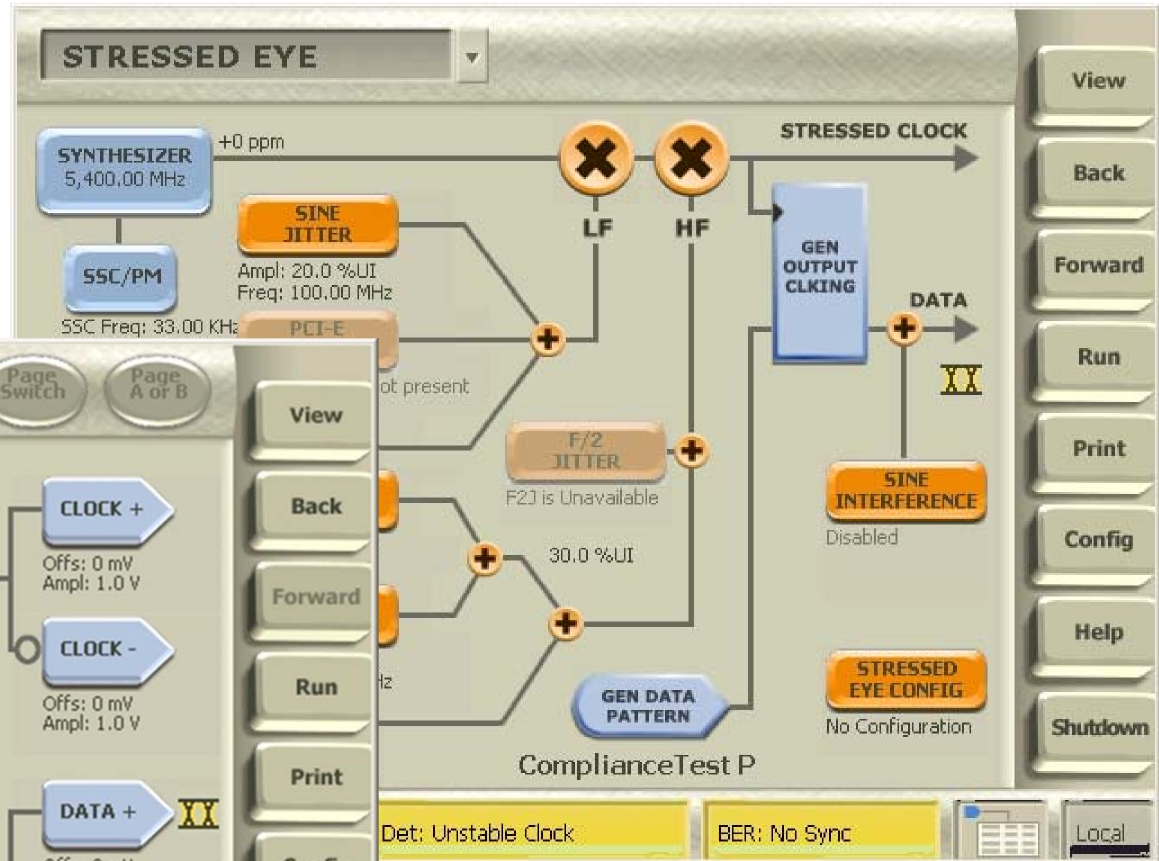
Typical Configuration

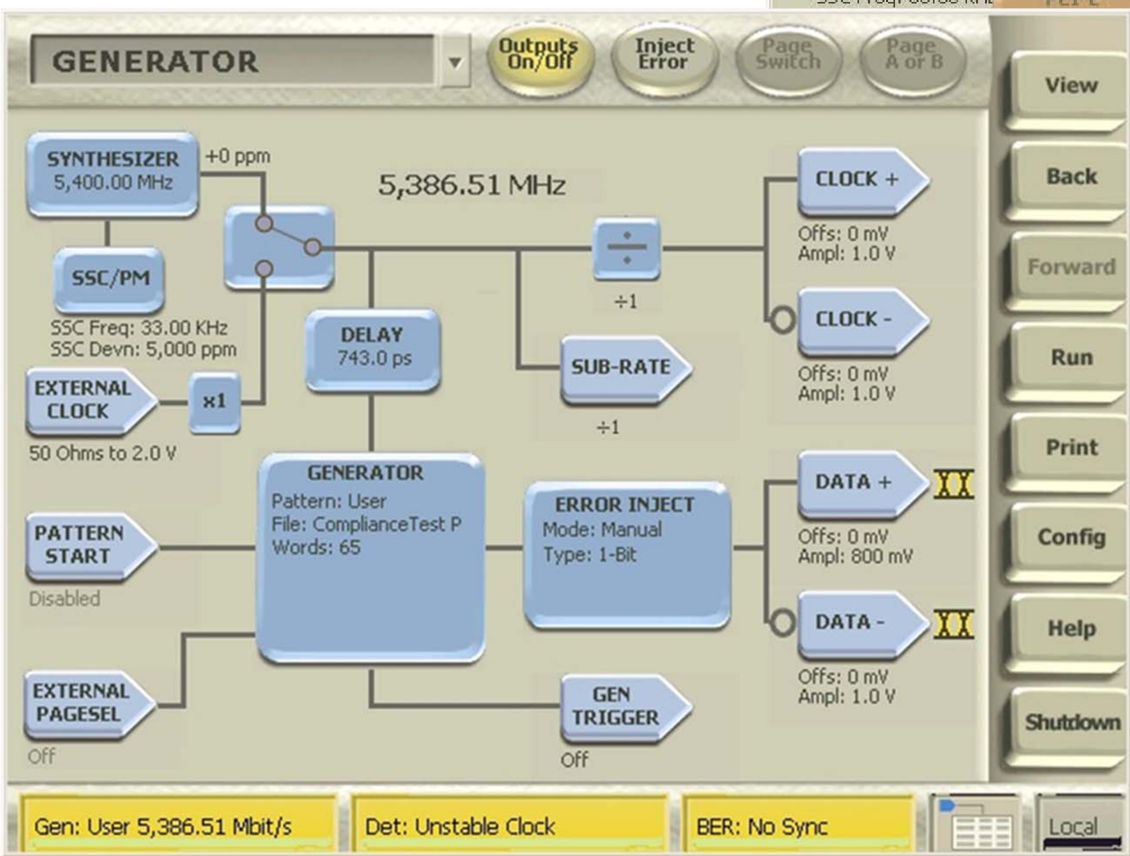
- BertScope BSA85C
  - Option STR
- BSA12500ISI
- DP-AUX
- TF-DP-TPA-PRC
  - Wilder DP Fixtures
- Misc:
  - Phase Matched Cables
  - TTC
  - Power Splitter



Two Tone SJ, with Stationary HFSJ Parked at 200 MHz.

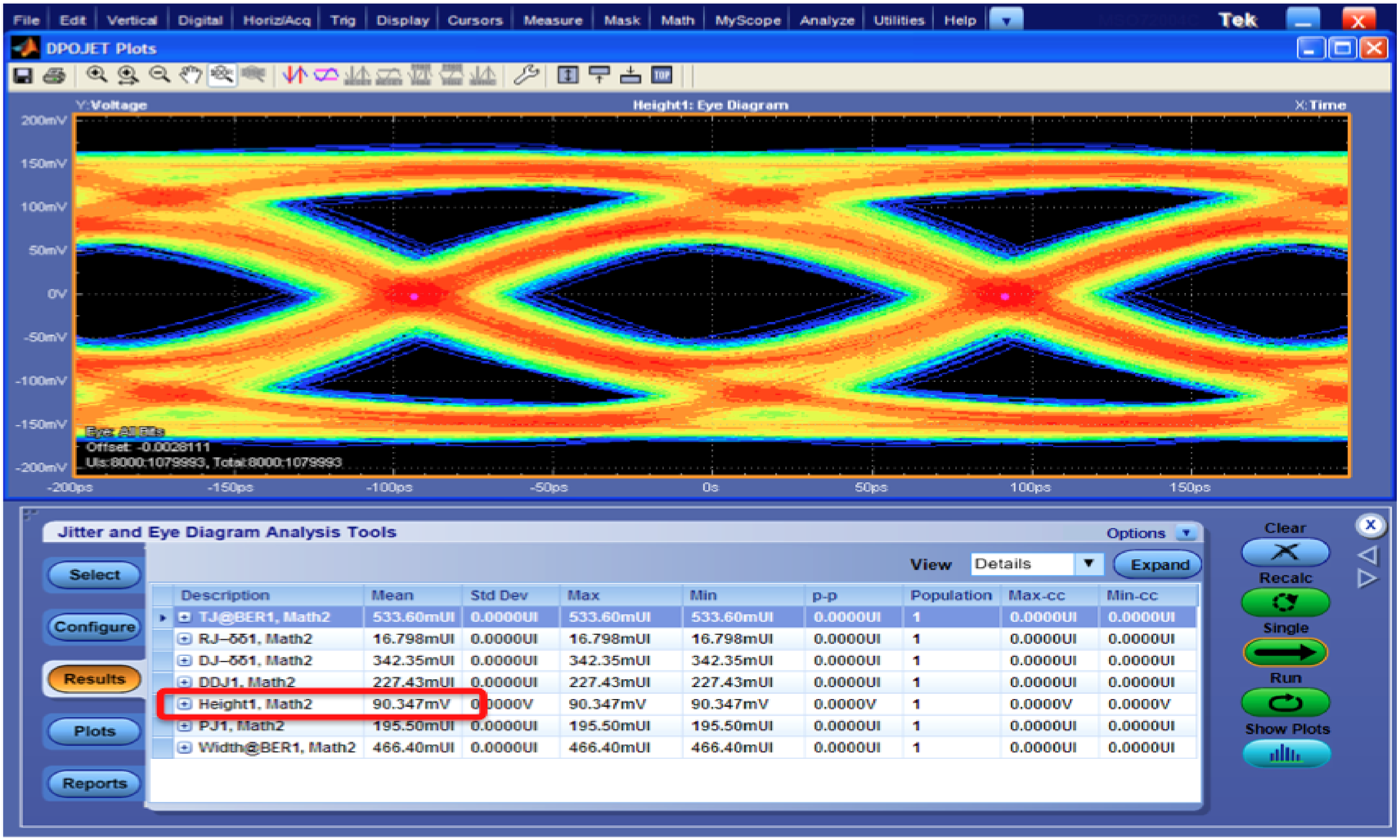
New HFSJ source for fixed 200 MHz SJ as required by DP1.2.



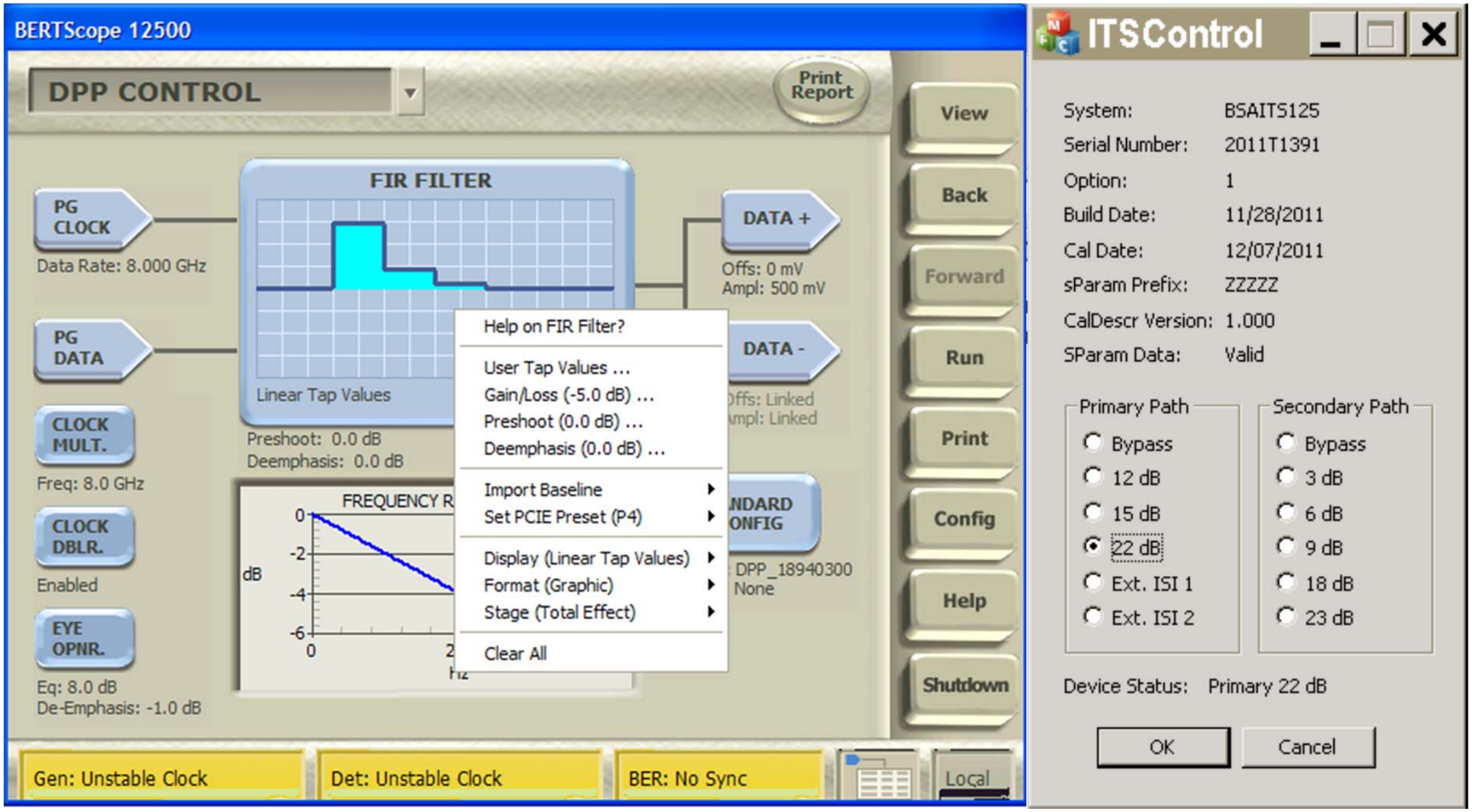


Generator page showing Patterns and capability of generation large amount Crosstalk with differential sub-rate Clock Outputs.

Realtime Scope confirmation of calibration specs (HBR2) in this case, with 640MHz Equalizer Zero



Data Dependent Jitter Variability
Introducing BSAITS (BertScope Accessory)



Through an automated selection of fixed ISI traces in the BSAITS instrument augmented with fine (mdB) controls the DPP FIR filter a continuously variable high precision ISI source is provided.

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DisplayPort 1.2
Sink (Rx) Test Observation Time

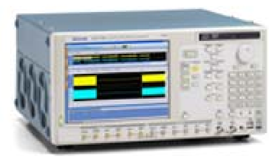
Four Principal Test Frequencies at 2, 10, 20 and 100 MHz SJ

Table 4-1: Test Parameters for BER Measurement

Data Rate	Jitter Frequency	Number of Bits	Max Num of Bit Errors Allowable	Observation Time[1] (seconds)	Data Rate Offset
HBR2 *HBR* *RBR*	*2 MHz*	10^{12}	*1000*	*HBR2 =185s* *HBR=370s* *RBR=620s*	*0*
HBR2 *HBR* *RBR*	*10 MHz*	10^{11}	*100*	*HBR2=19s* *HBR=37s* *RBR=62s*	*+350ppm* *+350ppm* *+350ppm*
HBR2 *HBR* *RBR*	*20 MHz*	10^{11}	*100*	*HBR2=19s* *HBR=37s* *RBR=62s*	*0*
HBR2 *HBR*	*100 MHz*	10^{11}	*100*	*HBR2=19s* *HBR=37s*	*0*

*To evaluate multiply number of bits by the unit interval in ps. (i.e. for HBR: 10^{11} bits at HBR = 370ps/UI * 10^{11} UI = 37 seconds*

Complete Tektronix DisplayPort Instrument Portfolio

Receiver/Sink Tests (Compliance) **DP-Sink**- Receiver jitter (synthesized ISI) and amplitude sensitivity compliance and margin test. To 6Gbps	**AWG7122B** with Opt.1, 6 and 8 SerialXpress Digital Signal Generation + DP-AUX controller + TekExpress DP-Sink SW (currently automates DP 1.1)	
Receiver/Sink Tests (Characterization) Receiver Silicon characterization and compliance testing capability to 26Gbps	**BSA125C** with JMAP and SSC and HW Options DPP 125A and CR125A provide support for future bit-rates (12-26G) with a unique portfolio of Scope and Bert combined features.	
DP Channel Tests Source and Sink electrical channel performance, Crosstalk, Impedance and return loss. High Dynamic Range instrument	**DSA8300** 80E10 TDR Sampling Module for DSA8200 Sampling Scope S-Parameter Analysis Software 80SICON Software	
Cable Tests Cable crosstalk, skew and frequency domain measurements, sdd21, sdd11.	**DSA8300** 4X 80E08 TDR Sampling Module for DSA8300 Sampling Scope	
Transmitter/Source Tests Signal timing stability and SSC analysis, Transmitter AC parametric, Jitter, Amplitude.	**DSA71254C** DPOJET Jitter Analysis software SMA Adapters TCA-SMA 2 per scope Differential SMA Probe P7313SMA (optional) + DP-AUX controller + DP12 (Sw Option)