Display Port Physical Layer Testing Challenges

Agilent Technologies Testing Overview

Jim Choate

Presentation Topics

Display Technologies Overview

Testing DisplayPort (TX focus)

DisplayPort Compliance Testing and Program

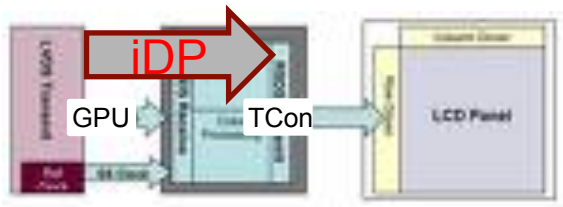
Agilent DisplayPort solutions

Overview: DisplayPort Technology

Computing

Consumer Electronics

Portables



MYDP

Standard DisplayPort

eDP

iDP

MYDP

Type	**Box-to-Box**	**One Unit (laptops, games)**	**LVDS replacement internal**	**Portable-to-TV**
Lanes	**1, 2, or 4**	**1, 2, or 4**	**4 or 8**	**1**
Bit Rate	**1.62, 2.7, 5.4**	**1.62, 2.7,5.4**	**3.24 or 3.78**	**1.62, 2.7,5.4**
Version	**V1.2**	**V1.3**	**V1.1**	**V1.0 d2**
Status	**Early Silicon**	**Newly Proposed CTS**	**Test Guideline**	**Silicon November**

DP Technology: Main Link Lanes

Silicon structures:

- Structure leveraged from PCI Express
- Implementable on sub 65nm process
- Termination Voltage must be <2volts (internal to IC)

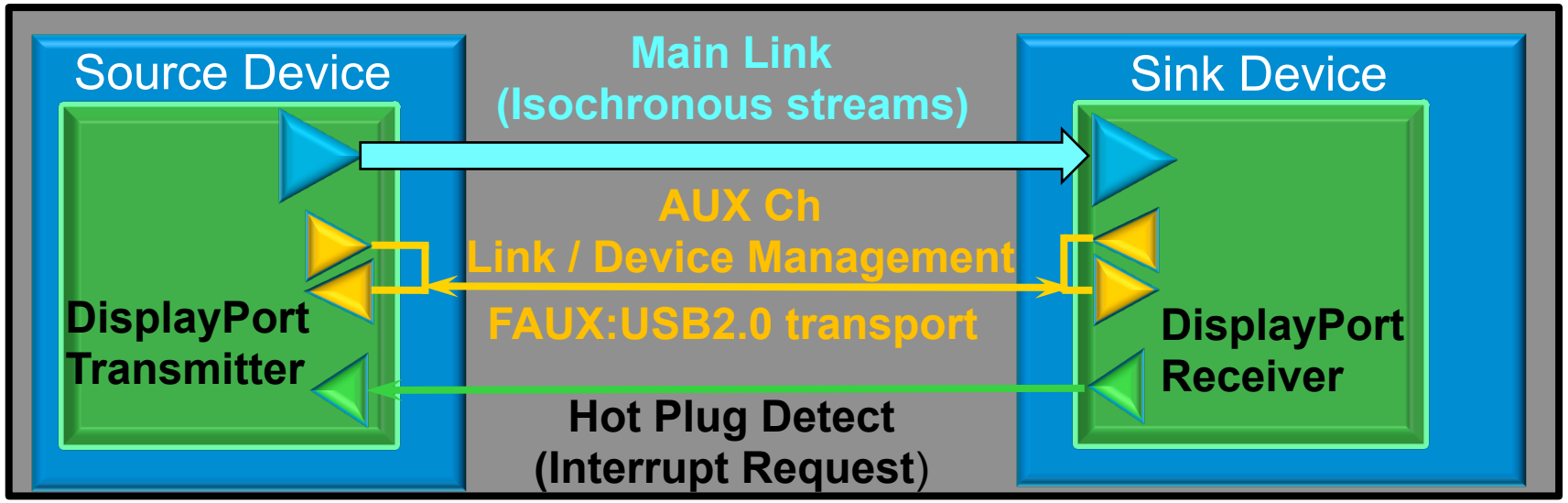
Receiver

- PLL BW=10MHz effective. Jitter tolerance curve specified.

Data Rate

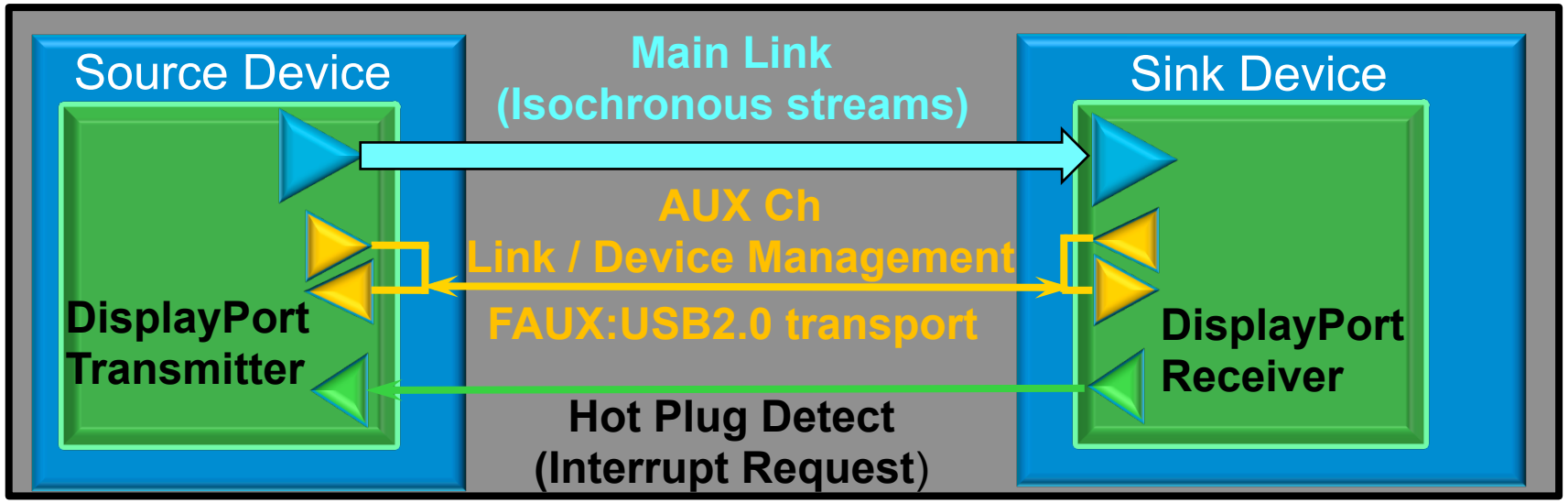
- 1.62 Gbs (RBR)
- 2.7 Gbs (HBR) [units supporting HBR must support RBR]
- 5.4Gbs (HBR2) [units supporting HBR2 must support HBR and RBR]

DisplayPort Technology: Interface Overview



- 1 to 4 unidirectional high speed lanes
  - Fixed data rate independent of display raster (refresh)
- Auxiliary channel for link communication and auxiliary data flow
  - Link Setup and Maintenance (1Mb/s - Manchester II)
  - USB 2.0 Transport (Fast AUX -540Mb/s - standard 8b/10b)
- Auto detect of cable plug/unplug

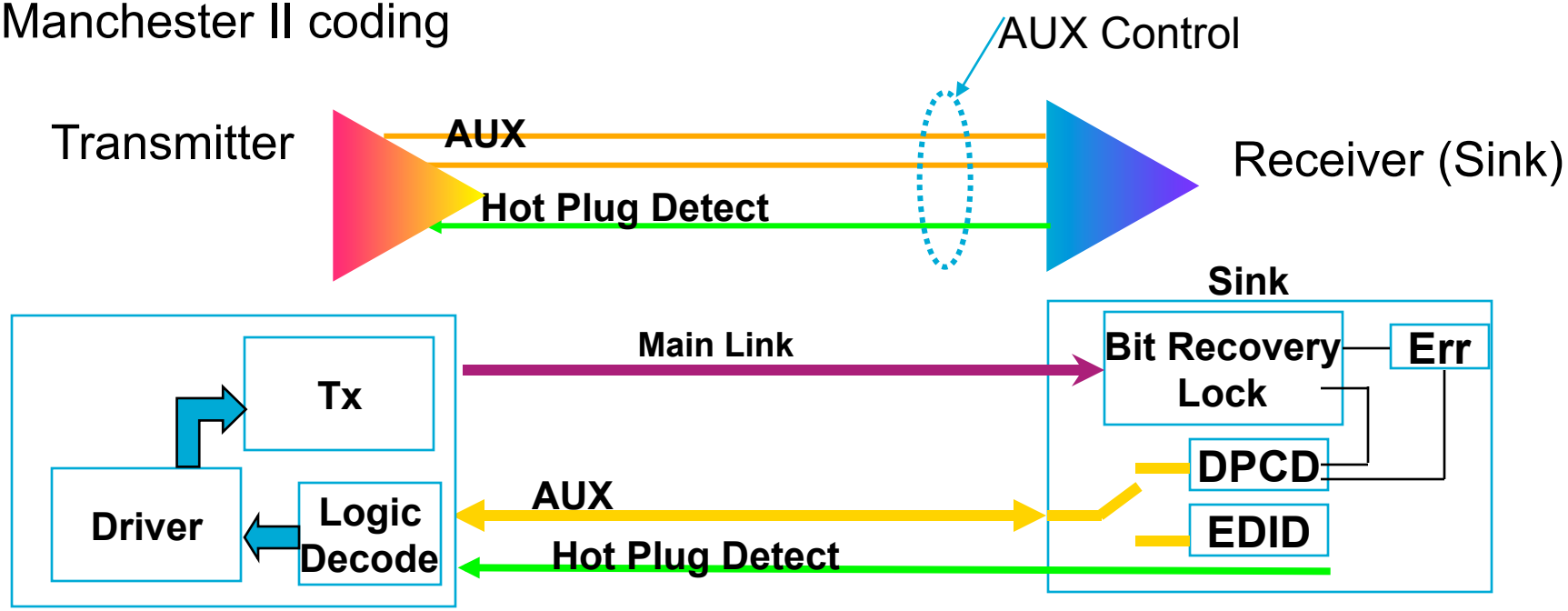
DisplayPort Technology: Interface Overview



- ❑ 3 Different Data Rates: 1.62, 2.7, 5.4 Gbs
- ❑ 4 Tx Level Settings: 400, 600, 800, 1200 mV (nominal)
- ❑ 4 Tx Pre Emphasis Settings: 0, 3.5, 6, 9.5 dB (nominal)
- ❑ 4 Tx Post Cursor Settings
- ❑ Optional Spread Spectrum Clocking

DP Technology: AUX Channel, DPCD

- Designated Control Link lane called ‘the AUX Channel’ specified. Operates at 1Mbs and is used in Link Training and Link Management and is Bidirectional Half Duplex.
- The Transmitter is the master.
- Receiver gains attention by pulling down on the Hot Plug Detect line.
- Manchester II coding



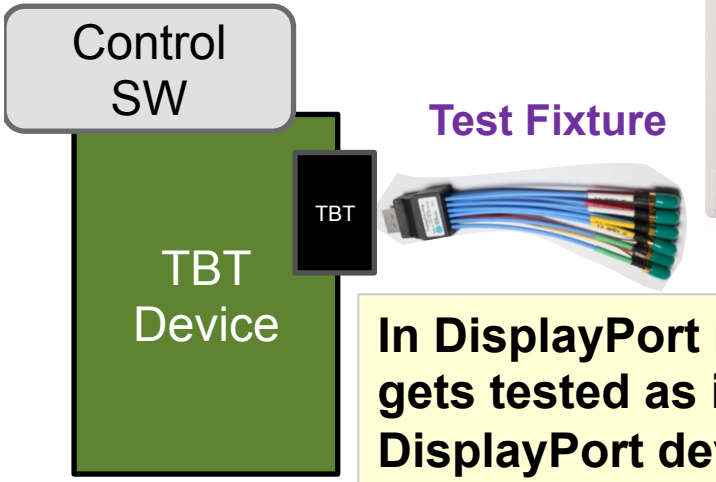
DisplayPort

Use Model

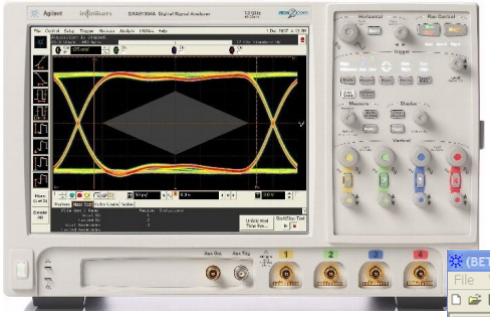
DisplayPort monitor

- ✓ **TBT switches to full DisplayPort mode**
- ✓ **All four lanes used to transport video**
- ✓ **DisplayPort compliance certification regimen applies**

Testing

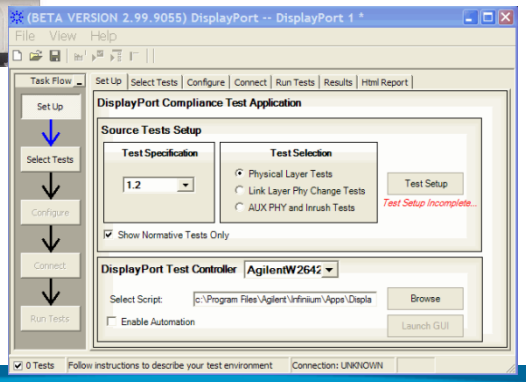


Test Fixture



Oscilloscope

DP Compliance SW



In DisplayPort mode… it merely gets tested as if it is a standard DisplayPort device with a mDP connector .

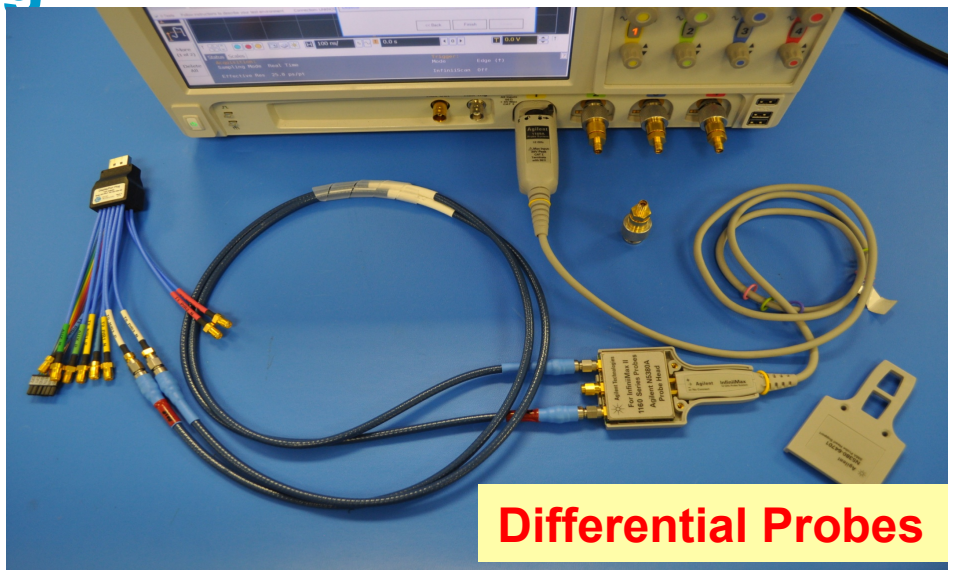
DisplayPort vs HDMI… a Comparison

	HDMI	DisplayPort
Market	HDTV/Gaming	PCs
Technology	TMDS (8B/10B)	PCI-Express/New (8B/10B)
Configuration	4 lanes (3 Data, 1 Ck) Differential, DC coupled	1, 2, or 4 lanes (Embedded Clock) Differential, AC coupled
Bit Rate	250Mbs to 3.4Gbs per lane	1.62, 2.7, or 5.4Gbs
Tx/Rx Negotiation	EDID/DDC	Aux Channel
Compliance	Authorized Test Centers	Qualified Test Houses
Ownership	HDMI.org	VESA
Std/Royalty	Closed/Yes	Open/No
Driving Need	HDTV and HDCP	Margin, embedded application
Models	External	External, internal,and Embedded

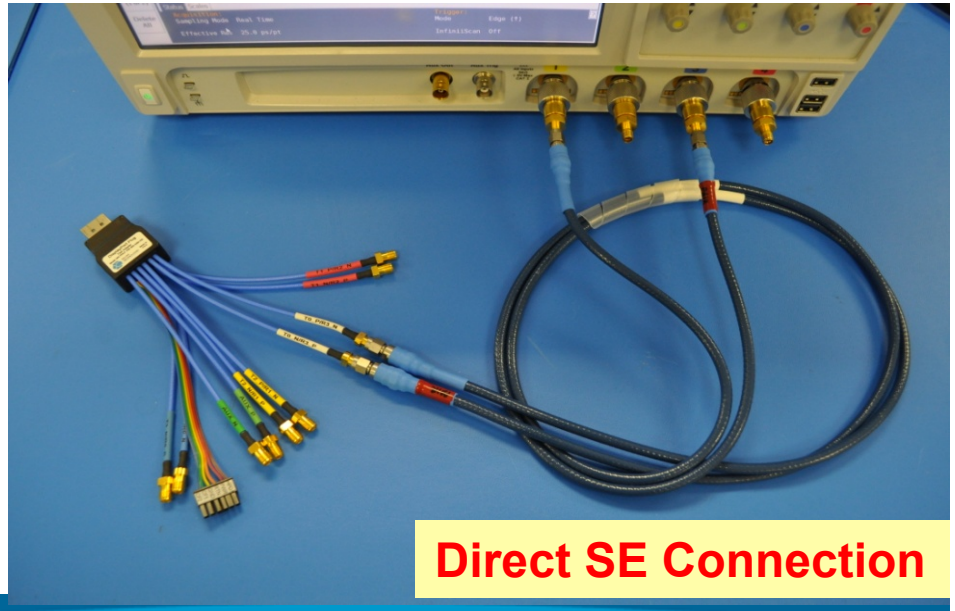
DisplayPort Source Testing

1. 3-1: Eye Diagram
2. 3-2: Level (Non PE)
3. 3-3: Pre-Emphasis Level
4. 3-4: Inter Pair Skew
5. 3-11: Non ISI Jitter
6. 3-12: RJ/ Total Jitter
7. 3-14: Main Link Frequency
8. 3-15: SSC Modulation Frequency
9. 3-16: SSC Modulation Depth

Differential

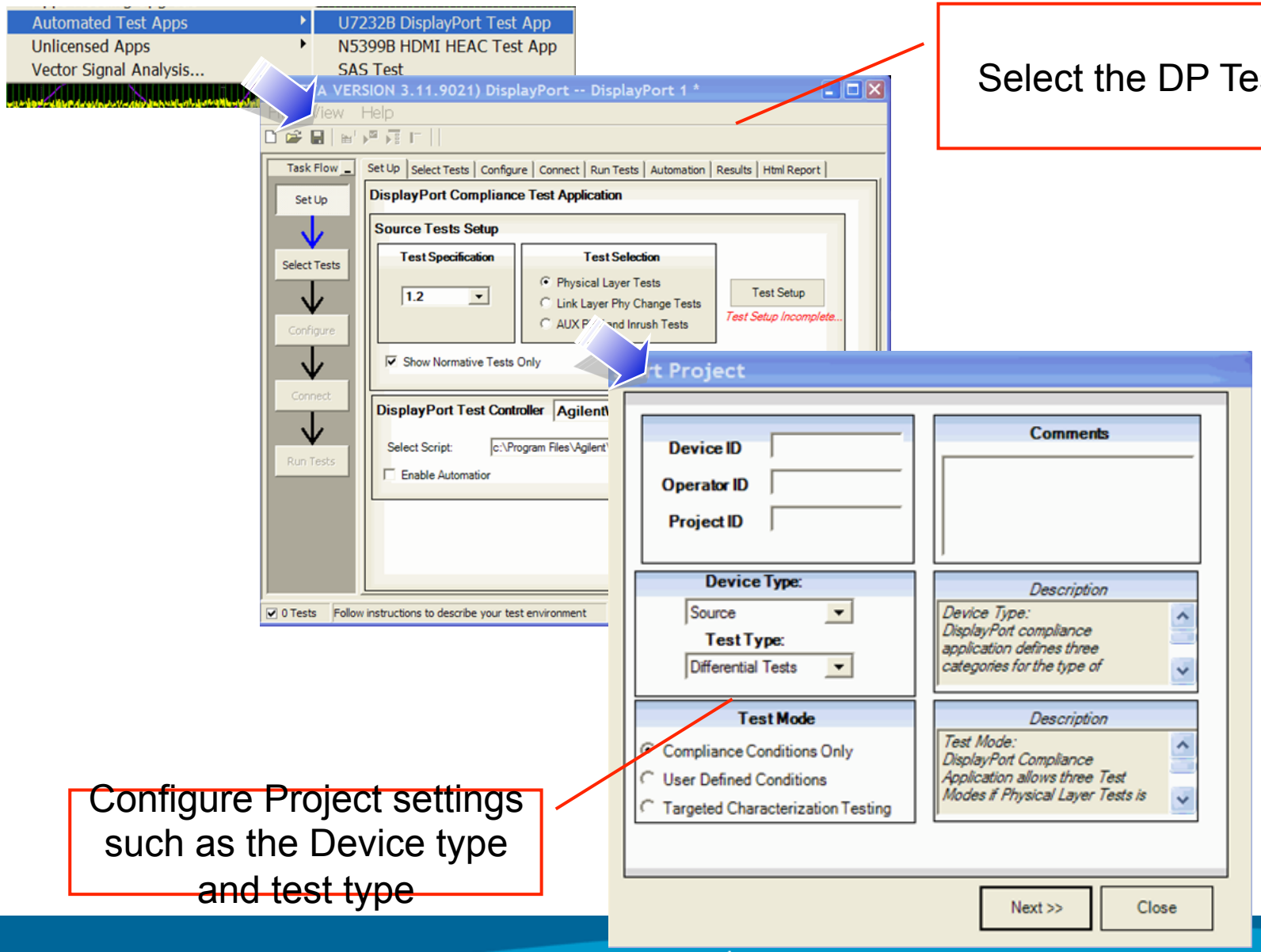


Differential Probes



Direct SE Connection

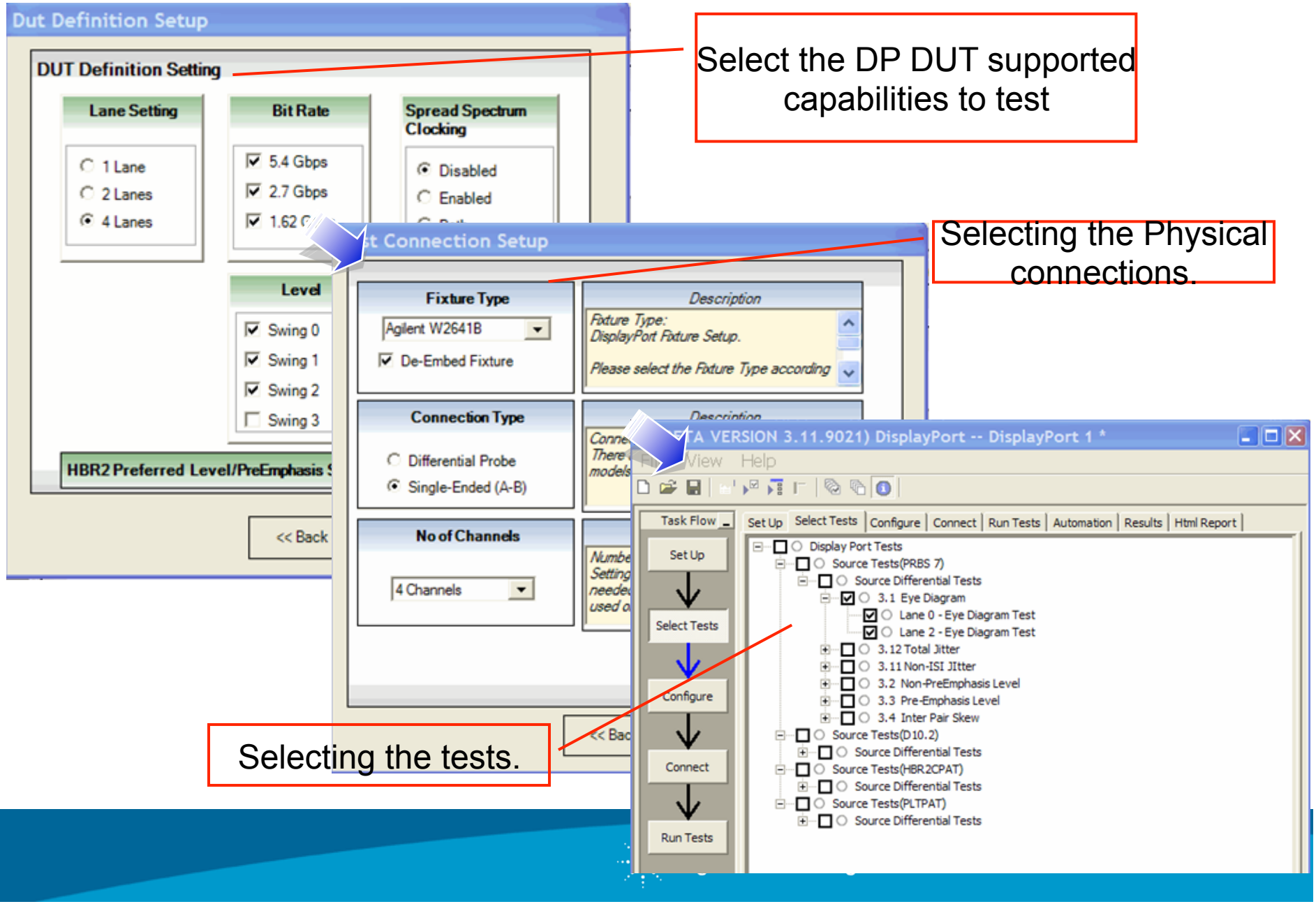
U7232B DP TX test sw speeds up testing (1)



Select the DP Test Setup

Configure Project settings such as the Device type and test type

Automated SW Speeds Up Testing (2)

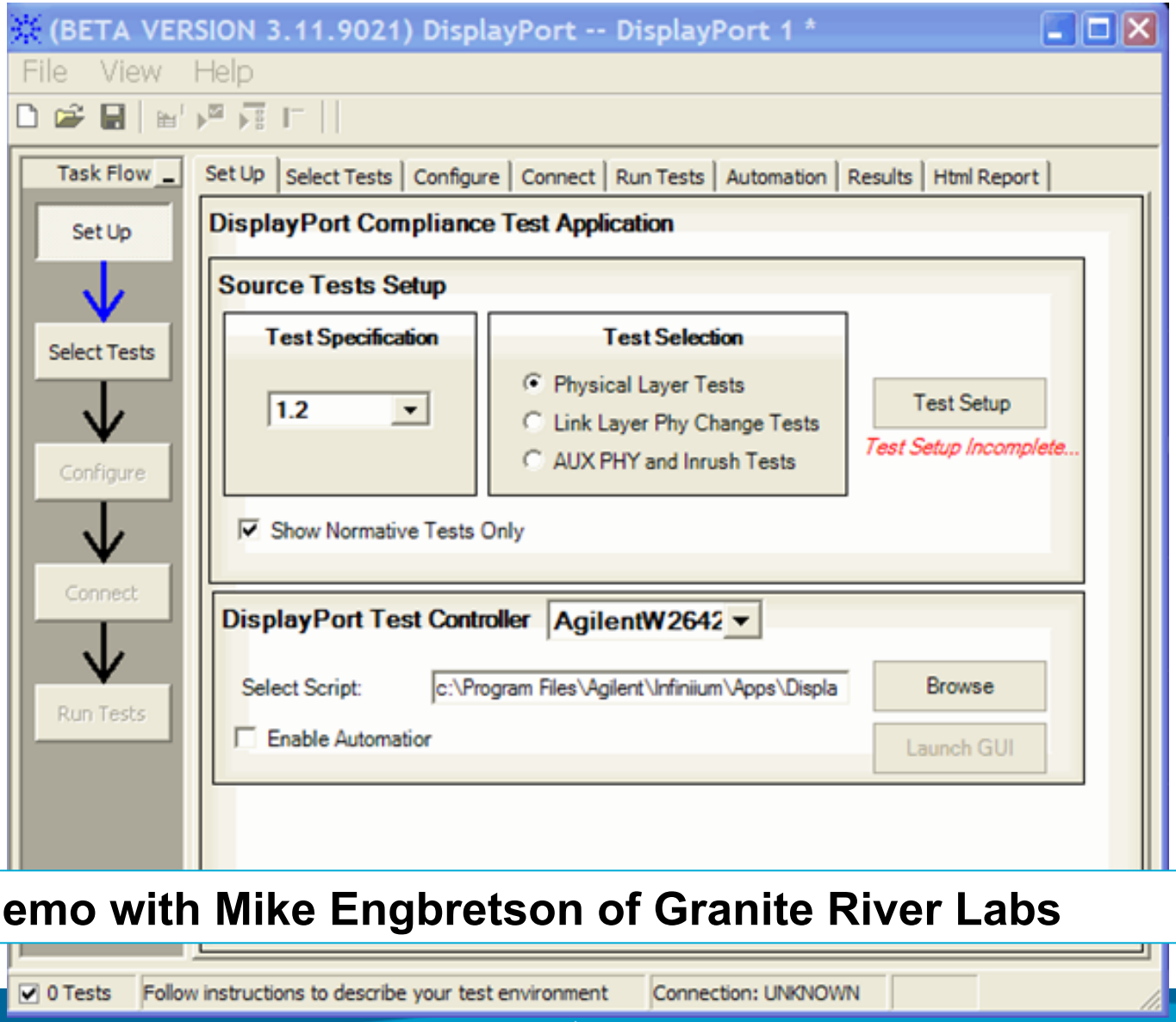


Select the DP DUT supported capabilities to test

Selecting the Physical connections.

Selecting the tests.

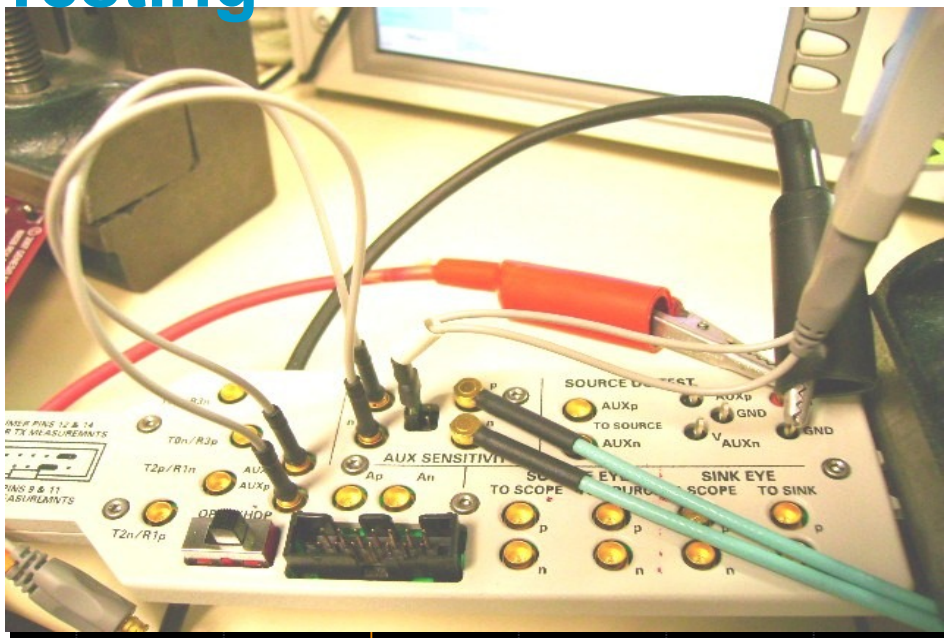
DP TX Test Demo

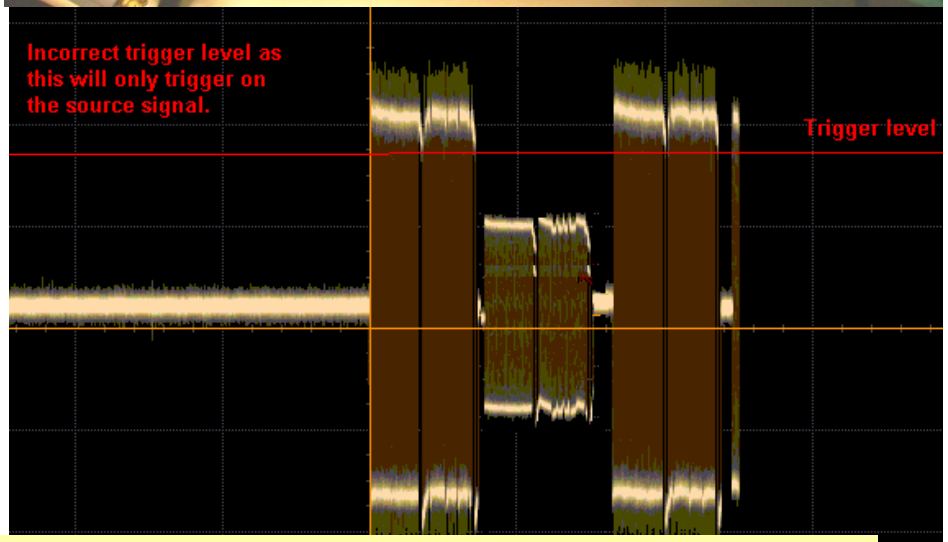


✓Demo with Mike Engbretson of Granite River Labs

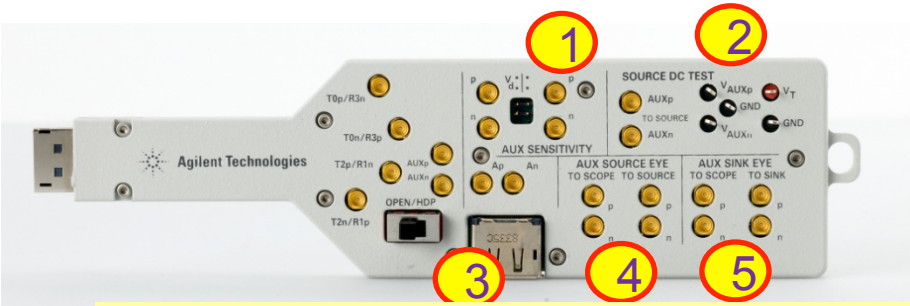
DisplayPort AUX Channel Testing

1. 8-1: AUX Eye Test
2. 8-2: AUX Sensitivity
3. 8-3: AUX- Termination
4. 8-4: AUX+ Termination
5. 8-5: Inrush Current





More tests coming for
Fast AUX mode



AUX Channel Testing added for CTS 1.1a but never made it to ATCs.

Testing DisplayPort Transmitters

Patterns Used:

- RBR/HBR: PRBS7 and D10.2
- HBR2: HBR2 CPAT: long pattern of coded 0's
  D10.2: (half clock)
  PLTPAT: ÷5 clock
  PCTPAT: 3x (5 ones, 5 zeros), 8x (1-1-0-0), 9x (1-0)

Test	Sub Item	Bit Rate	Pattern Required	Swing	PE	PC2	SSC	Lane
Eye Diagram								
	RBR	1.62	PRBS7	2	0	0	all	all
	HBR	2.7	PRBS7	2	0	0	all	all
	HBT (informative) embed channel CTLE	2.7	ComPat 2600	user	user	0	all	all
	HBR2 embed channel CTLE	5.4	ComPat 2600	user	user	0	all	all

Current TBT Only

Number of 'tests' : 3 data rates * 4 lanes * 2 SSC states=24 eye diagram tests

Actually the real number is 32 because HBR2 is tested twice!

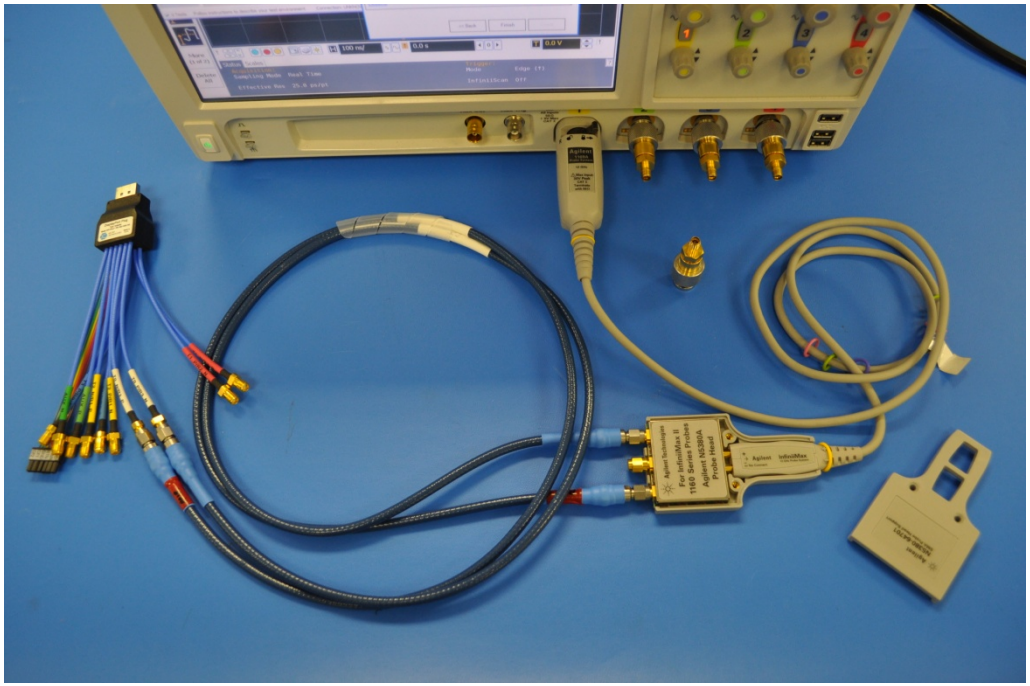
Testing

32 Total!

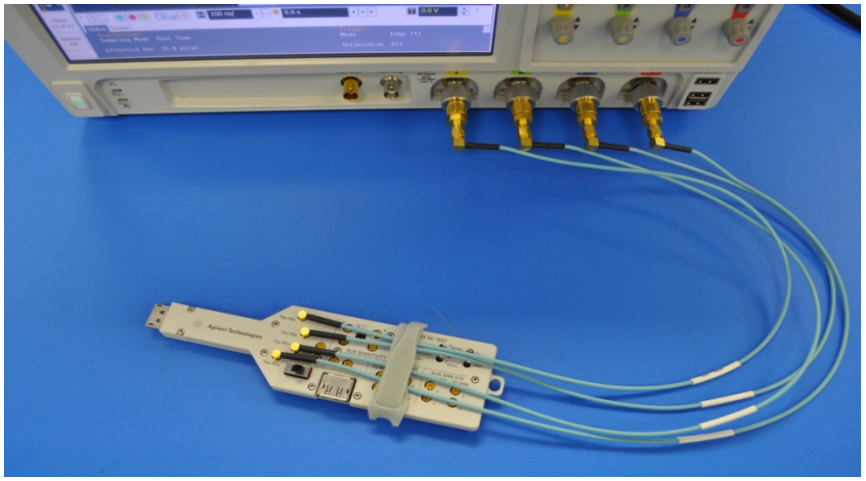
Test	Sub Item	Bit Rate	Pattern Required	Swing	PE	PC2	SSC	Lane
Eye Diagram								
	RBR	1.62	PRBS7	2	0	0	all	all
	HBR	2.7	PRBS7	2	0	0	all	all
	HBT (informative) embed channel CTLE	2.7	ComPat 2520	user	user	0	all	all
	HBR2 embed std channel CTLE	5.4	ComPat 2520	user	user	0	all	all
	HBR2 embed zero channel CTLE	5.4	ComPat 2520	user	user	0	all	all
Pre Emphasis Level Verification								
	RBR non transition 1	1.62	PRBS7	0	max between 0-3	0	all	all
	RBR non transition 2	1.62	PRBS7	1	max from 0-2	0	all	all
	RBR non transition 3	1.62	PRBS7	2	max of 0-1	0	all	all
	RBR 0 dB PreEmphasis	1.62	PRBS7	0	0	0	all	all
	RBR 0 dB PreEmphasis	1.62	PRBS7	1	0	0	all	all
	RBR 0 dB PreEmphasis	1.62	PRBS7	2	0	0	all	all
	RBR 0 dB PreEmphasis	1.62	PRBS7	3	0	0	all	all
	RBR PE Delta 0-1	1.62	PRBS7	0	0-1;	0	all	all
	RBR PE Delta 0-2	1.62	PRBS7	0	1-2;	0	all	all
	RBR PE Delta 0-3	1.62	PRBS7	0	2-3;	0	all	all
	RBR PE Delta 1-1	1.62	PRBS7	1	0-1;	0	all	all
	RBR PE Delta 1-2	1.62	PRBS7	1	1-2;	0	all	all
	RBR PE Delta 2-1	1.62	PRBS7	2	0-1	0	all	all

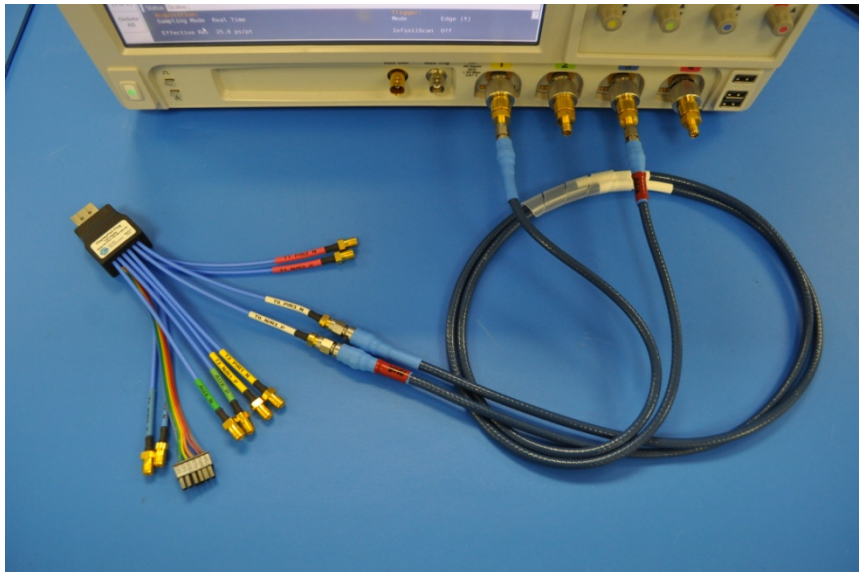
312 Total!

Source Test Setup (one lane)



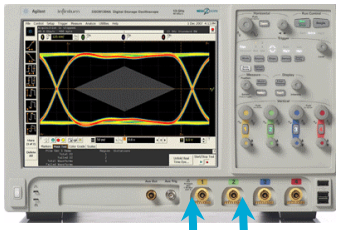
With Probe Amp and N5380A probe head

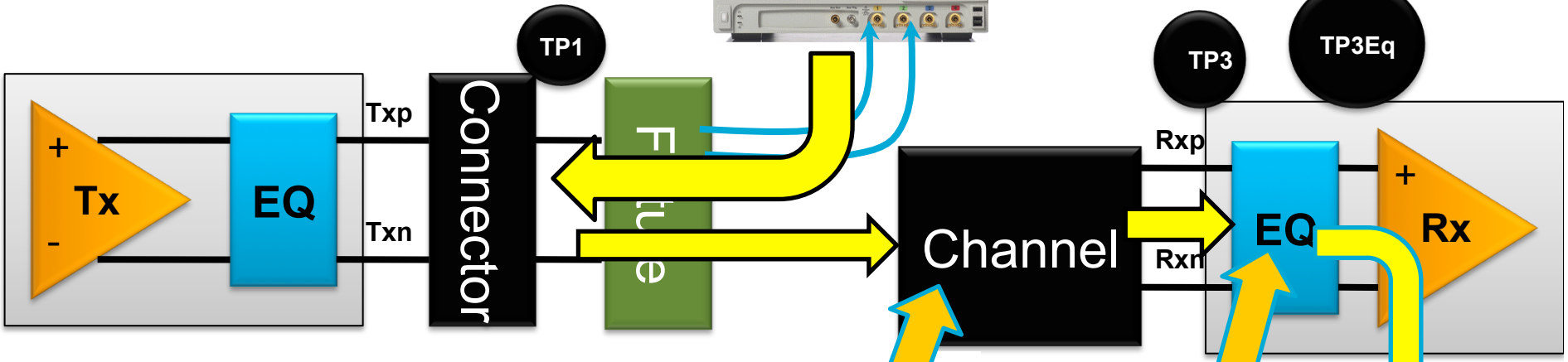




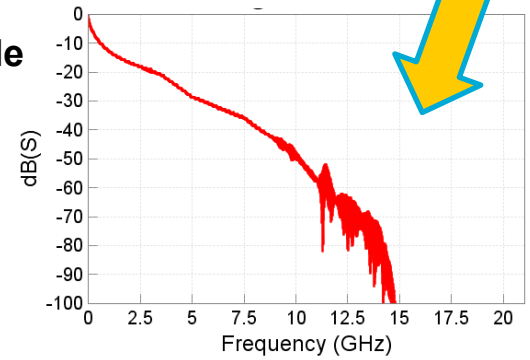
Direct A-B connection:
no probe Amp or probe head

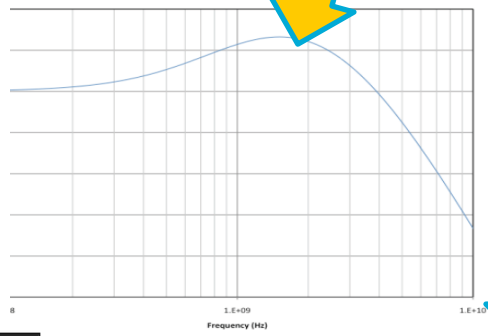
New for DP1.2: HBR2



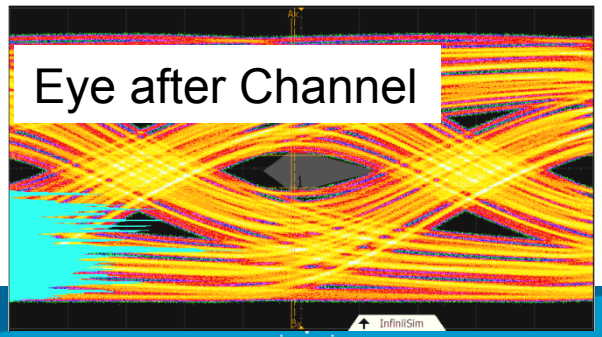


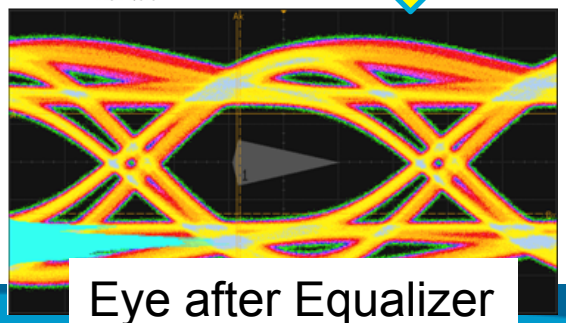
TP3Eq=TP2 Acquisition with Cable Model Embedded and Equalizer Applied. 10^{-9} BER





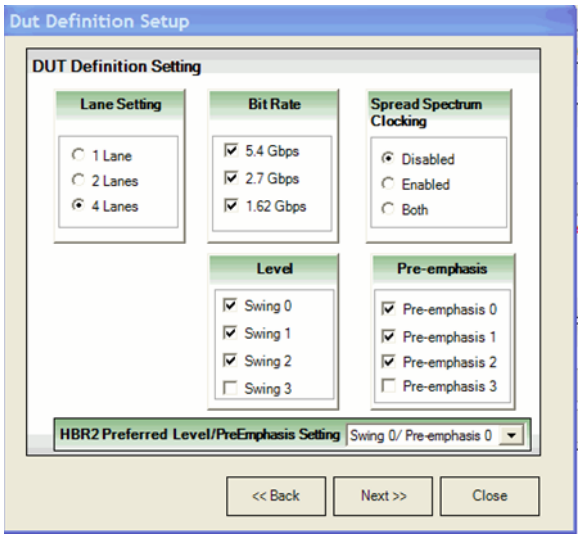
Equalizer: CTLE
DC Gain=1
Zero at 540MHz
Pole1=2.7GHz
Pole2=4.5GHz
Pole3=13 GHz
DUT state is user selectable





Display Port transmitter test challenges

- Transmitter test cases can be significant
- In the most complex case there are 100s of test cases
- Full test coverage of all test cases will take hours
- Determining test requirements for all required tests can be error prone if done manually



Agilent's answer to test challenges

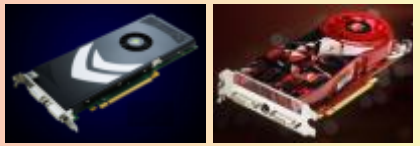
- User selects DUT attributes
- Compliance test sw will build a test plan
- Testing will progress through matrix
- If test is interrupted user can decide to continue where it stopped. All required tests will be selected and run by sw.

Common Failures/Issues

- Transmission path at 5.4Gbps
  - Hosts have the biggest challenge due to path length
  - At 5.4Gbps losses due to FR4 can hurt
  - Tuning for power consumption makes margins even tighter
- Aux channel SQ testing
  - Until now not much has been done here and many designs will have some signal quality issues
  - Causes interop issues, especially with long cables)
- Baseband/link layer support for testing
  - This is a HUGE issue. Many products are NOT testable due to no hw or sw support for test modes and/or aux channel controllers.

Agilent DisplayPort 1.2 Test Solutions

Source Test Solution



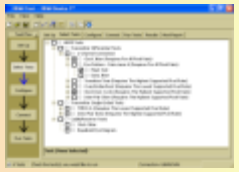
Computer Motherboards, ICs, Graphic Cards

DSO90000A Infiniium Real Time Oscilloscopes

W2642A

DPR-100

Automation



U7232B DisplayPort Compliance Test SW

W2641B

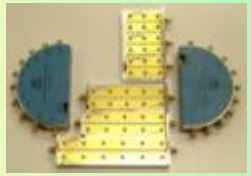
Wilder

TPA fixtures

Media Testing

Cables, PC Boards, Connectors

E5071C VNA Option TDR



BIT-DP-CBL-0002

Sink Test Solution

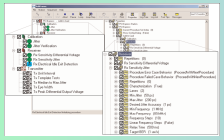
PC Monitors

N4915A -006 DP ISI Generation

N4903B JBERT

W2642A DPT-200

Automation



N5990A Rx Compliance Test SW

W2641B

Wilder/Bitifeye

TPA fixtures

Link Layer & General Solutions

HDCP, Link Layer Compliance Test, AUX Channel Validation and Test Pattern Generation

Available on the W2642A through Quantum Data upgrades or DPR-100/ DPT-200 through Unigraf upgrade

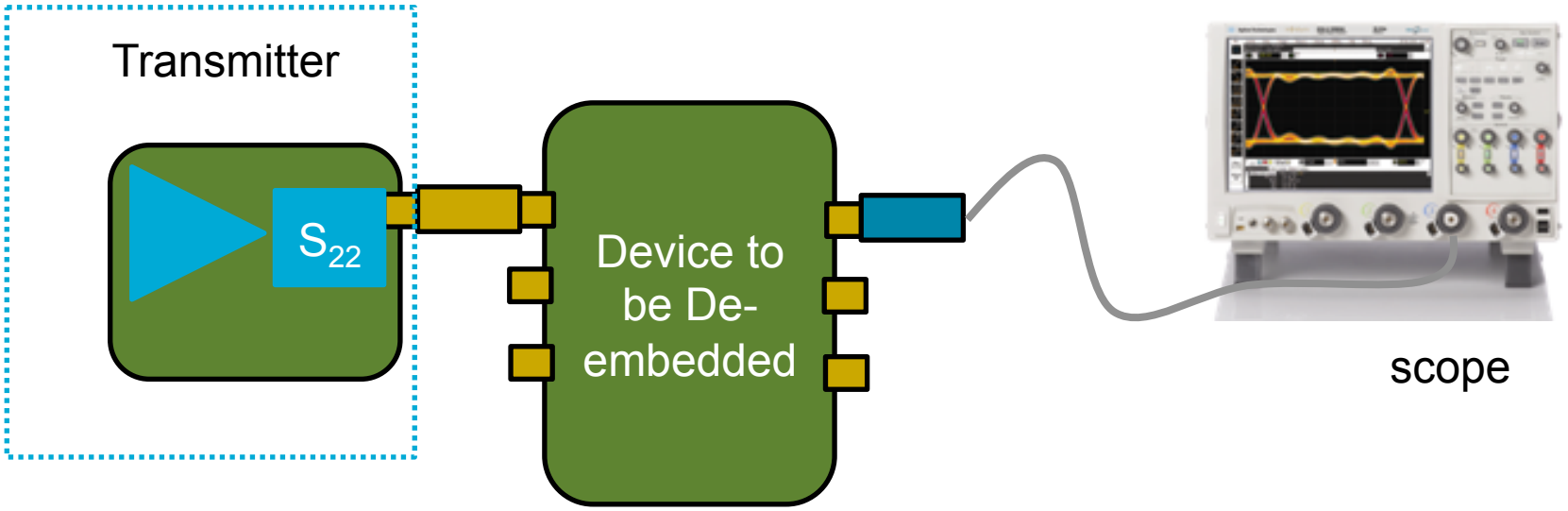
Main Link Analysis

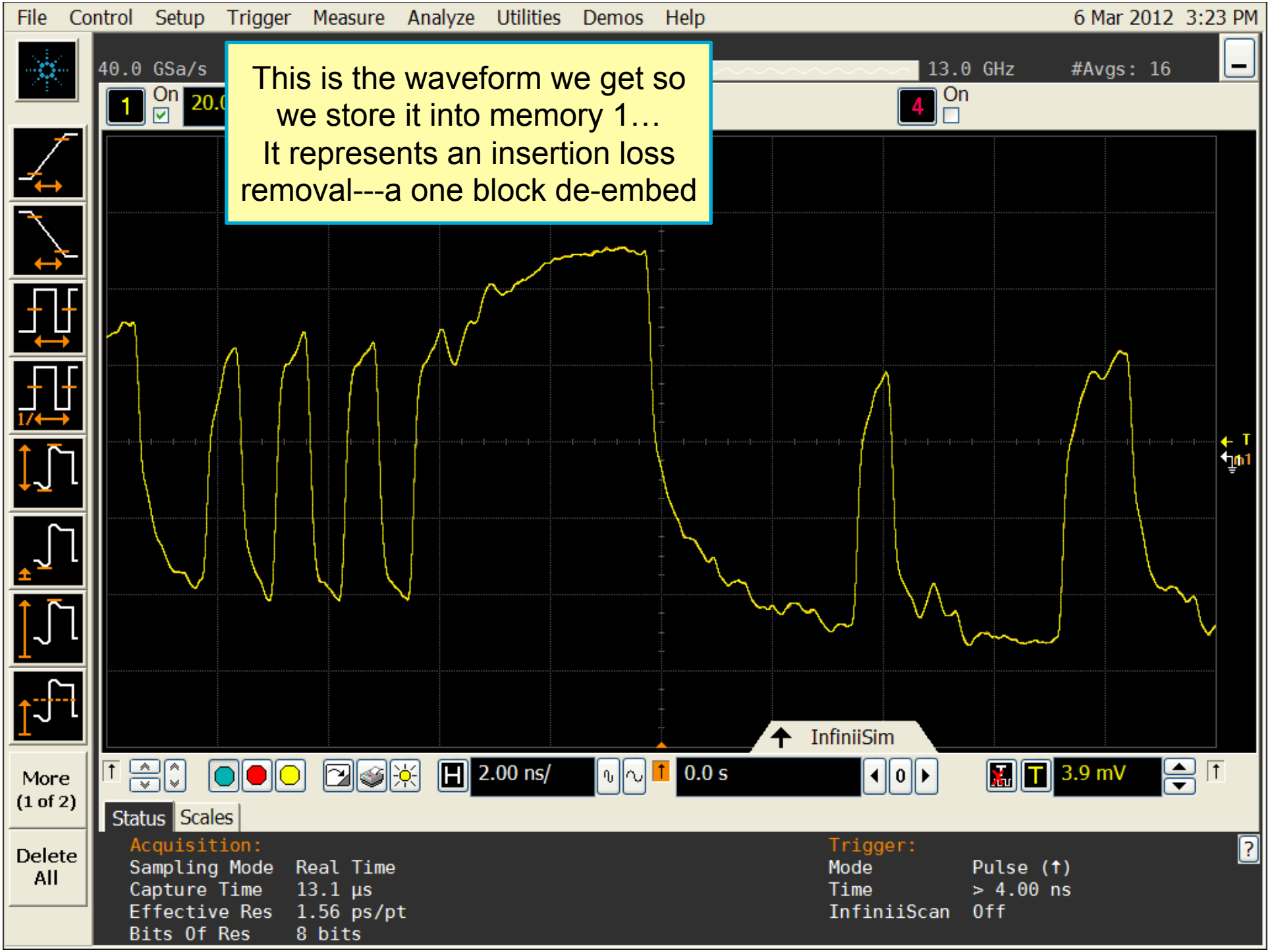
16900A w/FS4430

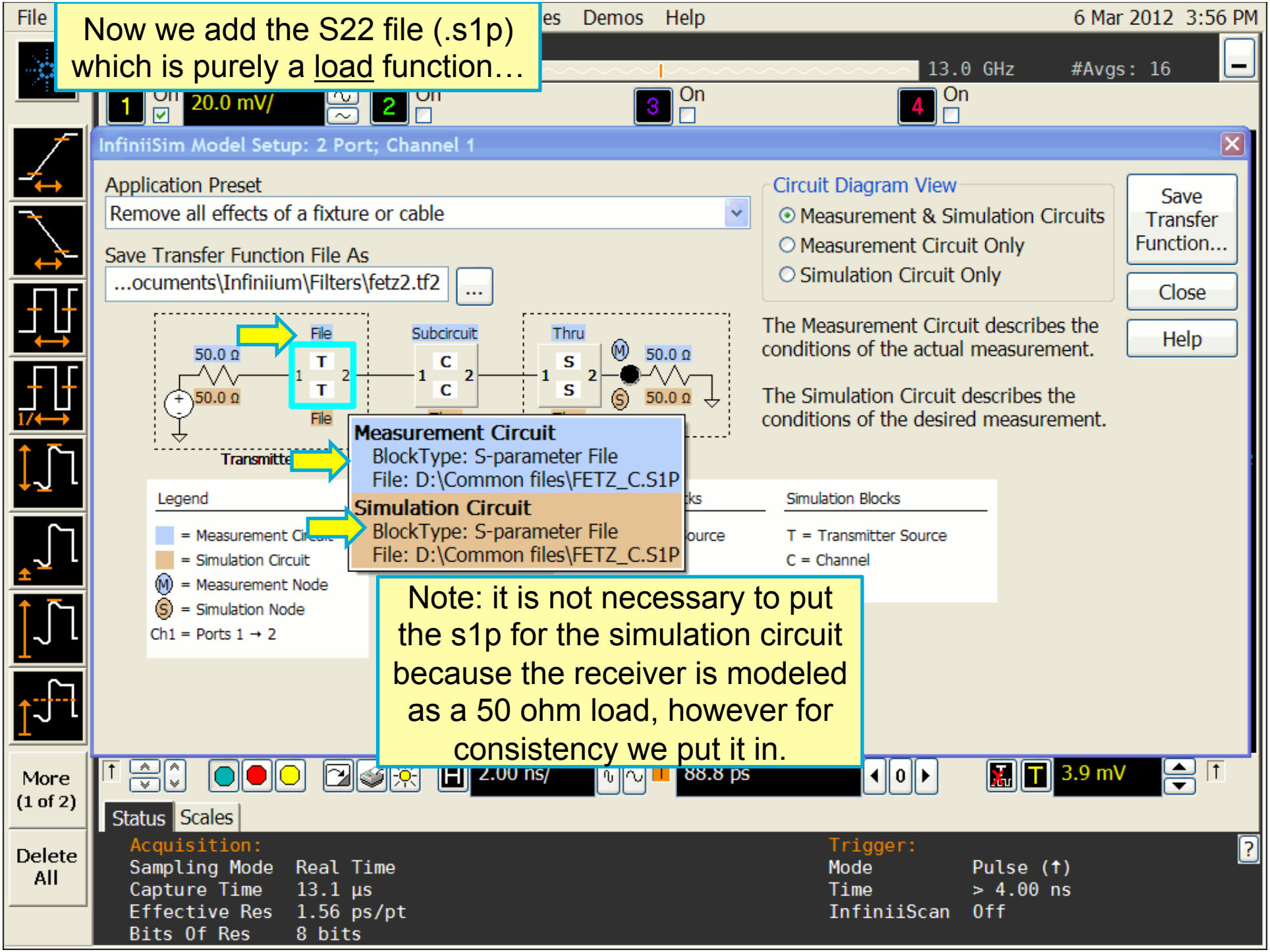
From FuturePlus

Another Measurement Issue: Realtime De-Embedding

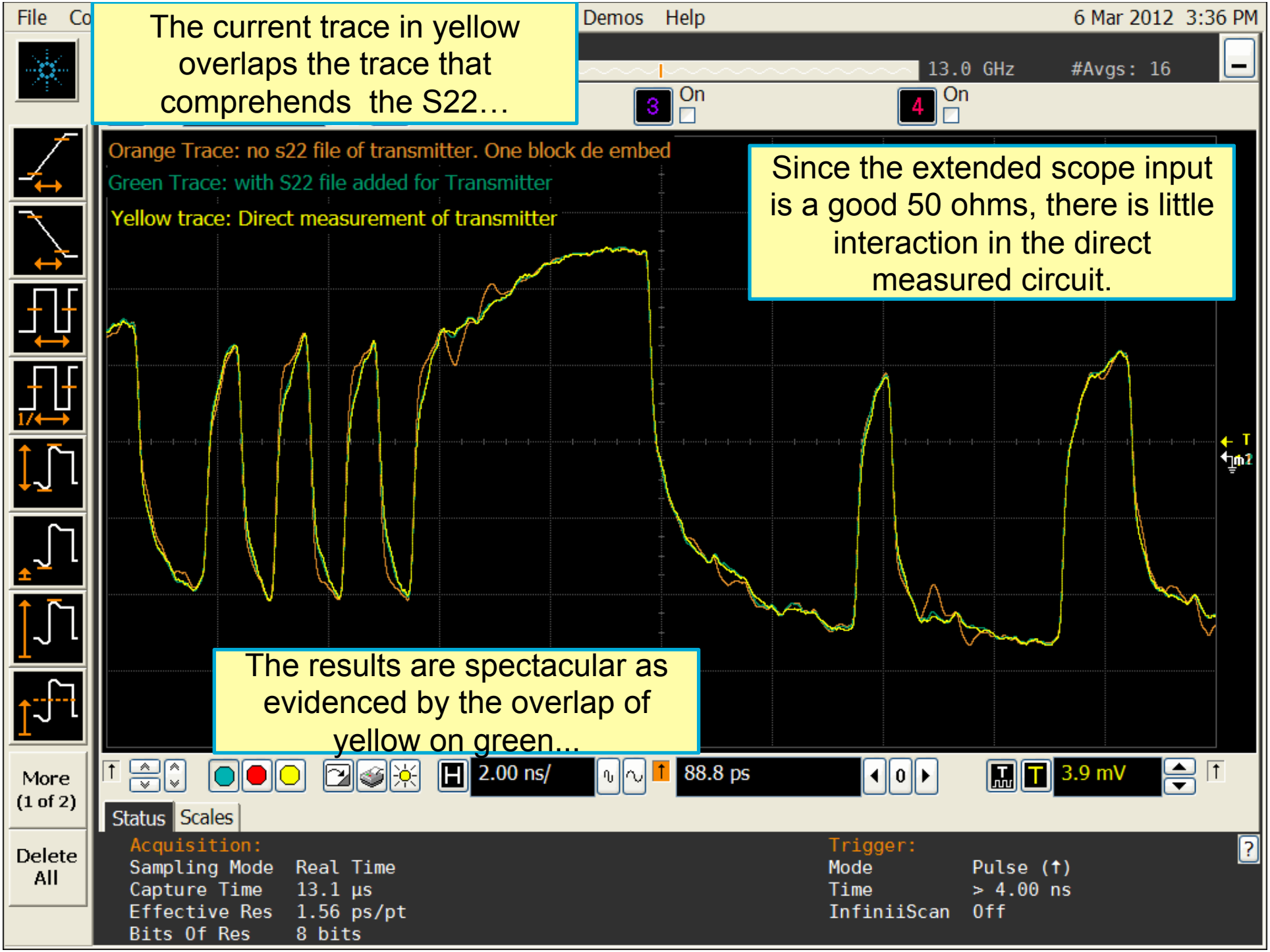
In performing a one block de-embed, the transmitter's output impedance is assumed to be 50 ohms. This assumption will disallow accounting for the interaction between the device to be de-embedded and the transmitter. This demo shows what the implications are and that InfiniiSim does account for interactions between blocks.




File Control Setup Trigger Measure Analyze Utilities Demos Help
6 Mar 2012 3:23 PM
40.0 GSa/s
13.0 GHz
#Avgs: 16
This is the waveform we get so we store it into memory 1…
It represents an insertion loss removal---a one block de-embed
1 On
4 On
InfiniiSim
2.00 ns/
0.0 s
3.9 mV
More (1 of 2)
Delete All
Status
Scales
Acquisition:
Sampling Mode Real Time
Capture Time 13.1 µs
Effective Res 1.56 ps/pt
Bits Of Res 8 bits
Trigger:
Mode Pulse (↑)
Time > 4.00 ns
InfiniiScan Off

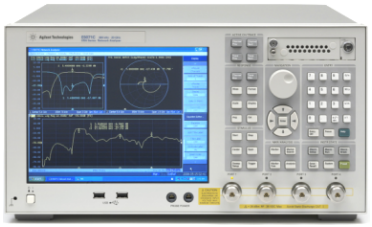

Now we add the S22 file (.s1p) which is purely a load function…
File
Demos
Help
6 Mar 2012 3:56 PM
13.0 GHz
#Avgs: 16
20.0 mV/
InfiniiSim Model Setup: 2 Port; Channel 1
Application Preset
Remove all effects of a fixture or cable
Save Transfer Function File As
...ocuments\Infiniium\Filters\fetz2.tf2
Circuit Diagram View
Measurement & Simulation Circuits
Measurement Circuit Only
Simulation Circuit Only
Save Transfer Function...
Close
Help
The Measurement Circuit describes the conditions of the actual measurement.
The Simulation Circuit describes the conditions of the desired measurement.
50.0 Ω
File
Subcircuit
Thru
Measurement Circuit
BlockType: S-parameter File
File: D:\Common files\FETZ_C.S1P
Simulation Circuit
BlockType: S-parameter File
File: D:\Common files\FETZ_C.S1P
Legend
= Simulation Circuit
= Measurement Node
= Simulation Node
Ch1 = Ports 1 → 2
Simulation Blocks
T = Transmitter Source
C = Channel
Note: it is not necessary to put the s1p for the simulation circuit because the receiver is modeled as a 50 ohm load, however for consistency we put it in.
More (1 of 2)
Delete All
2.00 ns/
88.8 ps
3.9 mV
Status
Scales
Acquisition:
Sampling Mode Real Time
Capture Time 13.1 µs
Effective Res 1.56 ps/pt
Bits Of Res 8 bits
Trigger:
Mode Pulse (↑)
Time > 4.00 ns
InfiniiScan Off


This is the waveform we get so we store it into memory 2…
File
Help
6 Mar 2012 3:33 PM
13.0 GHz
#Avgs: 16
1 On
2 On
3 On
4 On
Orange Trace: no s22 file of transmitter. One block de embed
Green Trace: with S22 file added for Transmitter
2.00 ns/
0.0 s
3.9 mV
More (1 of 2)
Delete All
Status
Scales
Acquisition:
Sampling Mode Real Time
Capture Time 13.1 µs
Effective Res 1.56 ps/pt
Bits Of Res 8 bits
Trigger:
Mode Pulse (↑)
Time > 4.00 ns
InfiniiScan Off

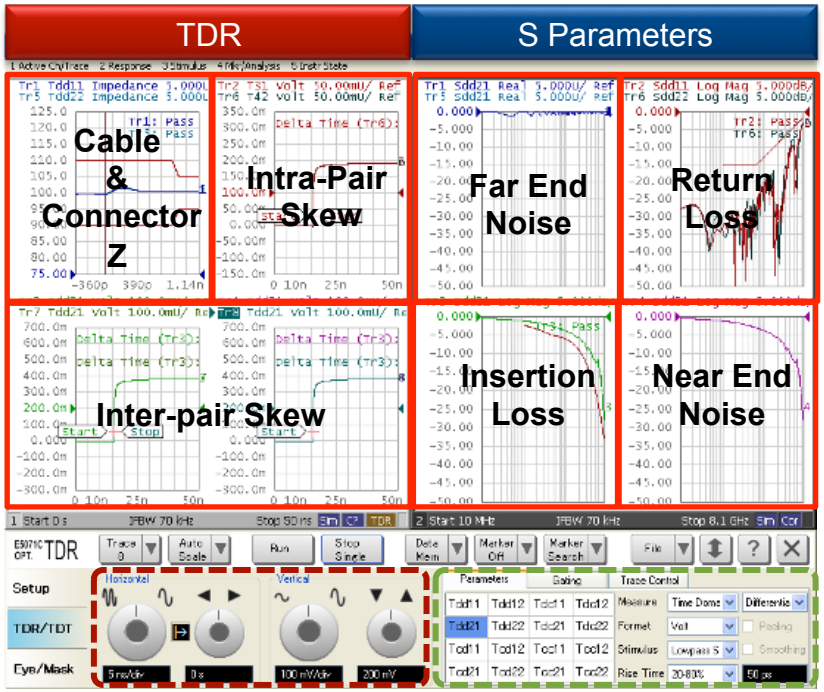

File Co
Demos Help
6 Mar 2012 3:36 PM
13.0 GHz
#Avgs: 16
3 On
4 On
The current trace in yellow overlaps the trace that comprehends the S22…
Orange Trace: no s22 file of transmitter. One block de embed
Green Trace: with S22 file added for Transmitter
Yellow trace: Direct measurement of transmitter
Since the extended scope input is a good 50 ohms, there is little interaction in the direct measured circuit.
The results are spectacular as evidenced by the overlap of yellow on green...
2.00 ns/
88.8 ps
3.9 mV
More (1 of 2)
Delete All
Status
Scales
Acquisition:
Sampling Mode Real Time
Capture Time 13.1 µs
Effective Res 1.56 ps/pt
Bits Of Res 8 bits
Trigger:
Mode Pulse (↑)
Time > 4.00 ns
InfiniiScan Off

Backup

One-box Solution for Cable/Connector Compliance Test

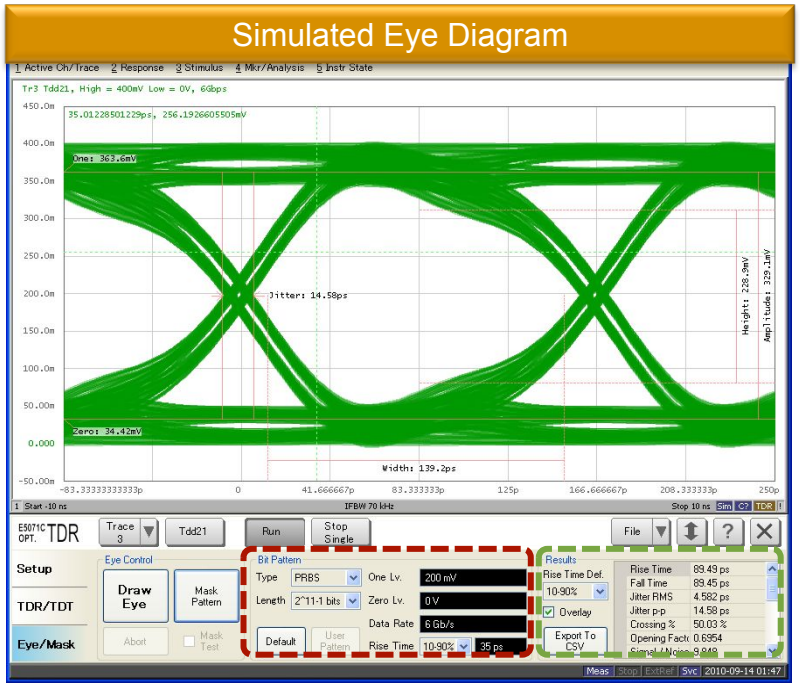


E5071C ENA Network Analyzer Option TDR



Horizontal / Vertical Controls

Parameter Selection



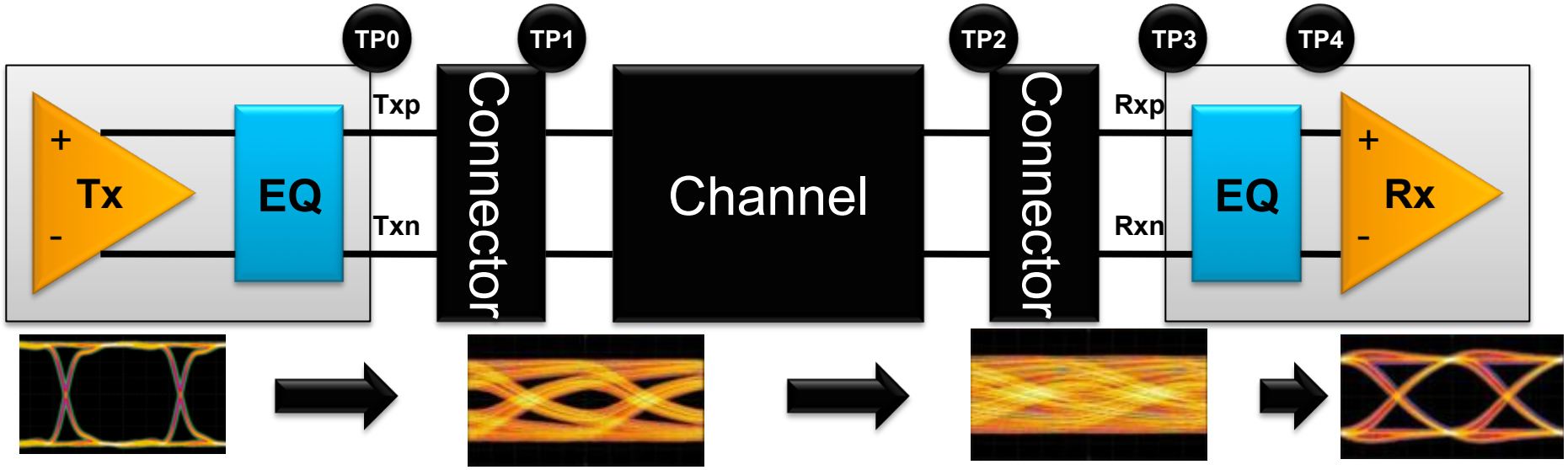
Virtual Bit Pattern Generator

Eye Result

- All required TDR and S parameters in **one screen** for completer device characterization
- Dedicated setup file for **FREE**
- Eye diagram simulation available **without additional** pattern generators

For more detail about the E5071C Option TDR, visit http://agilent.com/find/ena-tdr

Generalized Testing of High Speed Links



TP1: Interface Output of Transmitter

TP1-TP2: Cable Measurements

TP3: Tx through Cable
TP4: Tx through Cable and Eq

Transmitter	Cable	Receiver
Output Level	Loss vs Frequency	Sensitivity (Eye Height)
Eye Diagram		Eye Width
Jitter		
Skew	Skew	
PreEmphasis		Equalization
Frequency Accuracy		Lock Range

DP AUX Channel Validation

- New for compliance testing for DP 1.2
- Key operation for automation
- Key functionality for interoperability and interoperability testing
- Difficult to trigger on, acquire and present.