Presentation Topics

Display Technologies Overview
Testing DisplayPort (TX focus)
DisplayPort Compliance Testing and Program
Agilent DisplayPort solutions
Overview: DisplayPort Technology

<table>
<thead>
<tr>
<th>Type</th>
<th>Box-to-Box</th>
<th>One Unit (laptops, games)</th>
<th>LVDS replacement internal</th>
<th>Portable-to-TV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lanes</td>
<td>1, 2, or 4</td>
<td>1, 2, or 4</td>
<td>4 or 8</td>
<td>1</td>
</tr>
<tr>
<td>Bit Rate</td>
<td>1.62, 2.7, 5.4</td>
<td>1.62, 2.7, 5.4</td>
<td>3.24 or 3.78</td>
<td>1.62, 2.7, 5.4</td>
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<tr>
<td>Version</td>
<td>V1.2</td>
<td>V1.3</td>
<td>V1.1</td>
<td>V1.0 d2</td>
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<tr>
<td>Status</td>
<td>Early Silicon</td>
<td>Newly Proposed CTS</td>
<td>Test Guideline</td>
<td>Silicon November</td>
</tr>
</tbody>
</table>

**Agilent Technologies**
DP Technology: Main Link Lanes

Silicon structures:

- Structure leveraged from PCI Express
- Implementable on sub 65nm process
- Termination Voltage must be <2volts (internal to IC)

Receiver

- PLL BW=10MHz effective. Jitter tolerance curve specified.

Data Rate

- 1.62 Gbs (RBR)
- 2.7 Gbs (HBR) [units supporting HBR must support RBR]
- 5.4Gbs (HBR2) [units supporting HBR2 must support HBR and RBR]
### DisplayPort Technology: Interface Overview

- **1 to 4 unidirectional high speed lanes**
  - Fixed data rate *independent* of display raster (refresh)
- **Auxiliary channel for link communication and auxiliary data flow**
  - Link Setup and Maintenance (*1Mb/s - Manchester II*)
  - USB 2.0 Transport (*Fast AUX -540Mb/s - standard 8b/10b*)
- **Auto detect of cable plug/unplug**
DisplayPort Technology: Interface Overview

- 3 Different Data Rates: 1.62, 2.7, 5.4 Gbs
- 4 Tx Level Settings: 400, 600, 800, 1200 mV (nominal)
- 4 Tx Pre Emphasis Settings: 0, 3.5, 6, 9.5 dB (nominal)
- 4 Tx Post Cursor Settings
- Optional Spread Spectrum Clocking
DP Technology: AUX Channel, DPCD

- Designated Control Link lane called ‘the AUX Channel’ specified. Operates at 1Mbs and is used in Link Training and Link Management and is Bidirectional Half Duplex.
- The Transmitter is the master.
- Receiver gains attention by pulling down on the Hot Plug Detect line.
- Manchester II coding
DisplayPort

Use Model

TBT Device

TBT

DisplayPort monitor
✓ TBT switches to full DisplayPort mode
✓ All four lanes used to transport video
✓ DisplayPort compliance certification regimen applies

In DisplayPort mode... it merely gets tested as if it is a standard DisplayPort device with a mDP connector.

Testing

Control SW

TBT Device

TBT

Testing

Oscilloscope

DP Compliance SW

Test Fixture

Oscilloscope

In DisplayPort mode... it merely gets tested as if it is a standard DisplayPort device with a mDP connector.
# DisplayPort vs HDMI... a Comparison

<table>
<thead>
<tr>
<th></th>
<th>HDMI</th>
<th>DisplayPort</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Market</strong></td>
<td>HDTV/Gaming</td>
<td>PCs</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>TMDS (8B/10B)</td>
<td>PCI-Express/New (8B/10B)</td>
</tr>
<tr>
<td><strong>Configuration</strong></td>
<td>4 lanes (3 Data, 1 Ck)</td>
<td>1, 2, or 4 lanes (Embedded Clock)</td>
</tr>
<tr>
<td></td>
<td>Differential, DC coupled</td>
<td>Differential, AC coupled</td>
</tr>
<tr>
<td><strong>Bit Rate</strong></td>
<td>250Mbs to 3.4Gbs per lane</td>
<td>1.62, 2.7, or 5.4Gbs</td>
</tr>
<tr>
<td><strong>Tx/Rx Negotiation</strong></td>
<td>EDID/DDC</td>
<td>Aux Channel</td>
</tr>
<tr>
<td><strong>Compliance</strong></td>
<td>Authorized Test Centers</td>
<td>Qualified Test Houses</td>
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<tr>
<td><strong>Ownership</strong></td>
<td>HDMI.org</td>
<td>VESA</td>
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<tr>
<td><strong>Std/Royalty</strong></td>
<td>Closed/Yes</td>
<td>Open/No</td>
</tr>
<tr>
<td><strong>Driving Need</strong></td>
<td>HDTV and HDCP</td>
<td>Margin, embedded application</td>
</tr>
<tr>
<td><strong>Models</strong></td>
<td>External</td>
<td>External, internal, and Embedded</td>
</tr>
</tbody>
</table>
DisplayPort Source Testing

1. 3-1: Eye Diagram
2. 3-2: Level (Non PE)
3. 3-3: Pre-Emphasis Level
4. 3-4: Inter Pair Skew
5. 3-11: Non ISI Jitter
6. 3-12: RJ/ Total Jitter
7. 3-14: Main Link Frequency
8. 3-15: SSC Modulation Frequency
9. 3-16: SSC Modulation Depth
U7232B DP TX test sw speeds up testing (1)

Select the DP Test Setup

Configure Project settings such as the Device type and test type
Automated SW Speeds Up Testing (2)

Select the DP DUT supported capabilities to test

Selecting the Physical connections.

Selecting the tests.
DP TX Test Demo

Demo with Mike Engbrethson of Granite River Labs
DisplayPort AUX Channel Testing

1. 8-1: AUX Eye Test
2. 8-2: AUX Sensitivity
3. 8-3: AUX- Termination
4. 8-4: AUX+ Termination
5. 8-5: Inrush Current

More tests coming for Fast AUX mode

AUX Channel Testing added for CTS 1.1a but never made it to ATCs.
Testing DisplayPort Transmitters

Patterns Used:
- RBR/HBR: PRBS7 and D10.2
- HBR2: HBR2 CPAT: long pattern of coded 0’s
  - D10.2: (half clock)
  - PLTPAT: \( \div 5 \) clock
  - PCTPAT: 3x (5 ones, 5 zeros), 8x (1-1-0-0), 9x (1-0)

<table>
<thead>
<tr>
<th>Test</th>
<th>Bit Rate</th>
<th>Pattern Required</th>
<th>Swing</th>
<th>PE</th>
<th>PC2</th>
<th>SSC</th>
<th>Lane</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eye Diagram</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RBR</td>
<td>1.62</td>
<td>PRBS7</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>all</td>
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<tr>
<td>HBR</td>
<td>2.7</td>
<td>PRBS7</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>all</td>
<td>all</td>
</tr>
<tr>
<td>HBT (informative) embed channel CTLE</td>
<td>2.7</td>
<td>ComPat 2600</td>
<td>user</td>
<td>user</td>
<td>0</td>
<td>all</td>
<td>all</td>
</tr>
<tr>
<td>HBR2 embed channel CTLE</td>
<td>2.7</td>
<td>ComPat 2600</td>
<td>user</td>
<td>user</td>
<td>0</td>
<td>all</td>
<td>all</td>
</tr>
<tr>
<td>Current TBT Only</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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</table>

Number of ‘tests’: 3 data rates * 4 lanes * 2 SSC states = 24 eye diagram tests

Actually the real number is 32 because HBR2 is tested twice!
# Testing

<table>
<thead>
<tr>
<th>Test</th>
<th>Sub Item</th>
<th>Bit Rate</th>
<th>Pattern Required</th>
<th>Swing</th>
<th>PE</th>
<th>PC2</th>
<th>SSC</th>
<th>Lane</th>
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<tbody>
<tr>
<td><strong>Eye Diagram</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RBR</td>
<td></td>
<td>1.62</td>
<td>PRBS7</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>all</td>
<td>all</td>
</tr>
<tr>
<td>HBR</td>
<td></td>
<td>2.7</td>
<td>PRBS7</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>all</td>
<td>all</td>
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<tr>
<td>HBR (informative) embed channel CTLE</td>
<td></td>
<td>2.7</td>
<td>ComPat 2520</td>
<td>user</td>
<td>user</td>
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<td>all</td>
<td>all</td>
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<tr>
<td>HBR2 embed std channel CTLE</td>
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<td>5.4</td>
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<tr>
<td>HBR2 embed zero channel CTLE</td>
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<td>ComPat 2520</td>
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<td><strong>Pre Emphasis Level Verification</strong></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>RBR non transition 1</td>
<td></td>
<td>1.62</td>
<td>PRBS7</td>
<td>0</td>
<td>0-3</td>
<td>0</td>
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<tr>
<td>RBR non transition 2</td>
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<td>1.62</td>
<td>PRBS7</td>
<td>1</td>
<td>0-2</td>
<td>0</td>
<td>all</td>
<td>all</td>
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<tr>
<td>RBR non transition 3</td>
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<td>1.62</td>
<td>PRBS7</td>
<td>2</td>
<td>max of 0-1</td>
<td>0</td>
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<tr>
<td>RBR 0 dB PreEmphasis</td>
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<td>1.62</td>
<td>PRBS7</td>
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<td>RBR 0 dB PreEmphasis</td>
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<td>PRBS7</td>
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<td>0</td>
<td>all</td>
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<tr>
<td>RBR 0 dB PreEmphasis</td>
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<td>1.62</td>
<td>PRBS7</td>
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<td>0</td>
<td>all</td>
<td>all</td>
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<tr>
<td>RBR 0 dB PreEmphasis</td>
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<td>1.62</td>
<td>PRBS7</td>
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<td>0</td>
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<tr>
<td>RBR PE Delta 0-1</td>
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<td>1.62</td>
<td>PRBS7</td>
<td>0</td>
<td>0-1;</td>
<td>0</td>
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<td>all</td>
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<tr>
<td>RBR PE Delta 0-2</td>
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<td>PRBS7</td>
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<td>RBR PE Delta 0-3</td>
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<td>PRBS7</td>
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<td>2-3;</td>
<td>0</td>
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<td>all</td>
</tr>
<tr>
<td>RBR PE Delta 1-1</td>
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<td>1.62</td>
<td>PRBS7</td>
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<td>0-1;</td>
<td>0</td>
<td>all</td>
<td>all</td>
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<tr>
<td>RBR PE Delta 1-2</td>
<td></td>
<td>1.62</td>
<td>PRBS7</td>
<td>1</td>
<td>1-2;</td>
<td>0</td>
<td>all</td>
<td>all</td>
</tr>
<tr>
<td>RBR PE Delta 2-1</td>
<td></td>
<td>1.62</td>
<td>PRBS7</td>
<td>2</td>
<td>0-1;</td>
<td>0</td>
<td>all</td>
<td>all</td>
</tr>
</tbody>
</table>
Source Test Setup (one lane)

With Probe Amp and N5380A probe head

Direct A-B connection:
no probe Amp or probe head
New for DP1.2: HBR2

TP3Eq=TP2 Acquisition with Cable Model Embedded and Equalizer Applied. $10^{-9}$ BER

Equalizer: CTLE
DC Gain=1
Zero at 540MHz
Pole1=2.7GHz
Pole2=4.5GHz
Pole3=13 GHz
DUT state is user selectable
Display Port transmitter test challenges

- Transmitter test cases can be significant
- In the most complex case there are 100s of test cases
- Full test coverage of all test cases will take hours
- Determining test requirements for all required tests can be error prone if done manually

Agilent’s answer to test challenges

- User selects DUT attributes
- Compliance test sw will build a test plan
- Testing will progress through matrix
- If test is interrupted user can decide to continue where it stopped. All required tests will be selected and run by sw.
Common Failures/Issues

- Transmission path at 5.4Gbps
  - Hosts have the biggest challenge due to path length
  - At 5.4Gbps losses due to FR4 can hurt
  - Tuning for power consumption makes margins even tighter
- Aux channel SQ testing
  - Until now not much has been done here and many designs will have some signal quality issues
  - Causes interop issues, especially with long cables
- Baseband/link layer support for testing
  - This is a HUGE issue. Many products are NOT testable due to no hw or sw support for test modes and/or aux channel controllers.
## Agilent DisplayPort 1.2 Test Solutions

<table>
<thead>
<tr>
<th>Source Test Solution</th>
<th>Media Testing</th>
<th>Sink Test Solution</th>
<th>Link Layer &amp; General Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Computer Motherboards, ICs, Graphic Cards</td>
<td>Cables, PC Boards, Connectors</td>
<td></td>
<td>HDCP, Link Layer Compliance Test, AUX Channel Validation and Test Pattern Generation</td>
</tr>
<tr>
<td>DSO90000A Infinium Real Time Oscilloscopes</td>
<td>E5071C VNA Option TDR</td>
<td>N4915A -006 DP ISI Generation</td>
<td>Available on the W2642A through Quantum Data upgrades or DPR-100/DPT-200 through Unigraf upgrade</td>
</tr>
<tr>
<td>W2642A</td>
<td>BIT-DP-CBL-0002</td>
<td>N5990A Rx Compliance Test SW</td>
<td>Main Link Analysis 16900A w/FS4430 From FuturePlus</td>
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<tr>
<td>DPR-100 Automation</td>
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<tr>
<td>U7232B DisplayPort Compliance Test SW</td>
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<td>W2642A DPT-200 Automation</td>
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<td>W2641B</td>
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</tr>
<tr>
<td>TPA fixtures</td>
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<tr>
<td>Wilder</td>
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<td>W2641B</td>
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<td>TPA fixtures</td>
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<tr>
<td>Wilder/Bitifeye</td>
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</table>

W2641B
BIT-DP-CBL-0002
W2642A
DPT-200 Automation
N4915A -006
DP ISI Generation
N5990A Rx Compliance Test SW
W2642A
DPT-200 Automation
16900A w/FS4430 From FuturePlus

Agilent Technologies
Another Measurement Issue: Realtime De-Embedding

In performing a one block de-embed, the transmitter’s output impedance is assumed to be 50 ohms. This assumption will disallow accounting for the interaction between the device to be de-embedded and the transmitter. This demo shows what the implications are and that InfiniiSim does account for interactions between blocks.
This is the waveform we get so we store it into memory 1… It represents an insertion loss removal---a one block de-embed.
Now we add the S22 file (.s1p) which is purely a load function...

Note: it is not necessary to put the s1p for the simulation circuit because the receiver is modeled as a 50 ohm load, however for consistency we put it in.
This is the waveform we get so we store it into memory 2...
The current trace in yellow overlaps the trace that comprehends the S22...

Since the extended scope input is a good 50 ohms, there is little interaction in the direct measured circuit.

The results are spectacular as evidenced by the overlap of yellow on green...
Backup
One-box Solution for Cable/Connector Compliance Test

E5071C ENA Network Analyzer Option TDR

- All required TDR and S parameters in one screen for complete device characterization
- Dedicated setup file for FREE
- Eye diagram simulation available without additional pattern generators

For more detail about the E5071C Option TDR, visit http://agilent.com/find/ena-tdr
Generalized Testing of High Speed Links

TP1: Interface Output of Transmitter
TP1-TP2: Cable Measurements
TP3: Tx through Cable
TP4: Tx through Cable and Eq

<table>
<thead>
<tr>
<th>Transmitter</th>
<th>Cable</th>
<th>Receiver</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Level</td>
<td>Loss vs Frequency</td>
<td>Sensitivity (Eye Height)</td>
</tr>
<tr>
<td>Eye Diagram</td>
<td></td>
<td>Eye Width</td>
</tr>
<tr>
<td>Jitter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Skew</td>
<td>Skew</td>
<td></td>
</tr>
<tr>
<td>PreEmphasis</td>
<td></td>
<td>Equalization</td>
</tr>
<tr>
<td>Frequency Accuracy</td>
<td></td>
<td>Lock Range</td>
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</tbody>
</table>

Agilent Technologies
DP AUX Channel Validation

- New for compliance testing for DP 1.2
- Key operation for automation
- Key functionality for interoperability and interoperability testing
- Difficult to trigger on, acquire and present.

Incorrect trigger level as this will only trigger on the source signal.

AUX signal Probing
HPD switch
Eye Test sections
AUX lane Termination Test section
AUX jumper
DP connection to other device i.e. like Aux Controller