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DP CTS Update and Overview

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GRL Chief Technology Engineer
April 30, 2012

Agenda

- GRL Introduction
- VESA Specification Version Numbers
- DP 1.2 CTS Test Requirements
- Transition from DP1.2 to DP1.2a Specification Preview

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DisplayPort Version Numbers

- Only one DisplayPort Standard specification version number active at any given time
  - With the publication of DisplayPort Standard Specification Ver.1.2 in JAN 2010, Specification Ver.1.1a document was retired

- As for DPCD Revision Number (at DPCD Address 00000h), multiple revision numbers may co-exist
  - When people casually refer to a “DP1.1a” product, they actually mean a DP device supporting DPCD Revision Number 1.1 only

DisplayPort Standard Version Number *(continued)*

- Link and PHY Compliance Test Specifications following DisplayPort Standard Version Number
  - Ver.1.1a available
    - *NOTE: Link CTS Ver.1.1b with addition of audio transport test to be published in DEC 2010 ~ JAN 2010*
  - Phase 1 of Ver.1.2 covering some of the additional features in DisplayPort1.2 (e.g., HBR2, Audio HBR) going to GMR (General Membership Review) in DEC 2010 ~ JAN 2011

- Other DP-derivative standards (eDP and iDP) have their own version numbers
  - eDP Standard Ver.1.2 published in MAY 2010
  - iDP Standard Ver.1.0 published in APR 2010

VESA | DisplayPort

DisplayPort 1.2 Compliance Testing

- VESA Test Implementation Task Group has been formed to manage transition from DP1.1a to DP1.2 test program with regards to qualifying test solutions – Mike E. Chairman, Bob Crepps Vice-Chair.
- Some DP 1.2 source and sink products have already been tested and certified under DP1.2 requirements with agreed upon test plan between test lab and Bob Crepps.
- GRL recommends you test to the DP 1.2(a) requirements
  - As a manufacturer, you will want to know if you meet DP1.2 requirements.
  - Sink PHY testing must follow DP1.2a CTS requirements due to CTS issue
  - If failures occur but pass DP 1.1a, you can still get approved under DP1.1a program until DP1.2 program is in place.

DisplayPort 1.2 Compliance Testing

- DP devices supporting only RBR/HBR are tested to DP 1.2 CTS since some RBR/HBR test items were updated in CTS 1.2
  - Testing of RBR/HBR is sometimes referred to as 'DP 1.2 Core'
- DP logo does not differentiate between 1.1a or 1.2 or any feature differences.
  - Example: a Sink that supports RBR/HBR carries the same logo as one that supports HBR2.

DisplayPort 1.2 Compliance Testing

	Applicable Reference Document and Section				
Device Type (Reference Section in this document)	**PHY CTS**	**Link CTS**	**EDID CTS**	**Interop CTS**	**Other**
3.3 - Source	3, 8	4	3	3	
3.4 - Sink	4, 8	5	4	3	
3.5 - Repeater	3, 4, 8	6		3	
3.6 - Legacy-to-DisplayPort Converter	3, 8	6		3	
3.7 - DisplayPort-to-Legacy Converter	4, 8	6		3	
3.8 - Replicator	3, 4, 8	6		3	
3.9 - Output Switch	3, 4, 8	6		3	
3.10 - Input Switch	3, 4, 8	6		3	
3.11 - Composite Sink	3, 4, 8	6		3	
3.12 – Passive Cable	5				
3.13 – Active Cable	9				
3.14 – Dual-mode Cable Adaptor					Dual-mode Cable Adaptor CTS
3.15 – Hybrid Device	6	5		3	

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DisplayPort 1.2 Compliance Testing

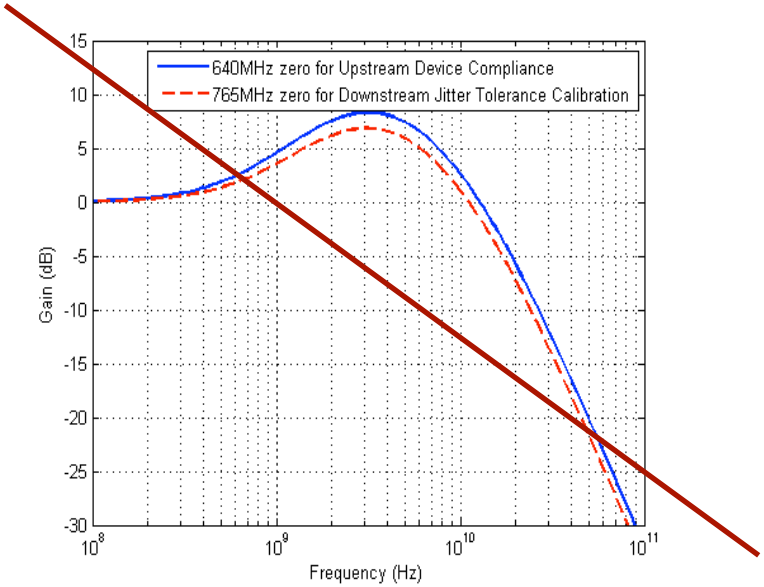
- DP 1.2 Major Test Items
  - 1.2 PHY RBR/HBR/HBR2
    - Source Electrical: Realtime Scope (Tek and Agilent)
    - Sink Electrical: AWG, BertScope, or J-BERT
  - 1.1b Link Layer Test
  - Link Negotiation Testing for HBR2
  - EDID
  - Interoperability (Various sources, sinks, cables)
    - Refer to Interop CTS for list
  - Other 1.2 functionality tested based on plan mutually agreed upon with DP Compliance Chair (Bob Crepps) and GRL
- DP ++ Major Test Items
  - Dual Mode Eye Diagram Measurement to be added

DP1.2a DP Specification Preview

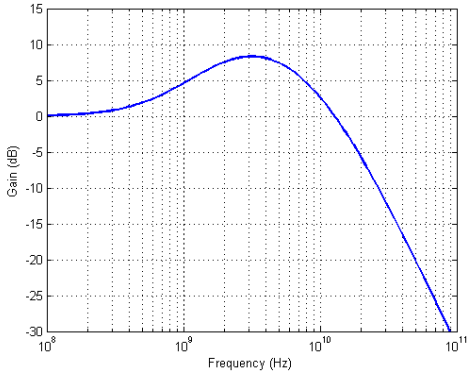
- Equalizer Changes for HBR and HBR2
  - In order to rationalize the Jitter and Eye Margins from TP1 > TP2 > TP3 > TP3_Eq, new Equalizer values were defined.
  - Specification change impacts DP1.2 PHY CTS, requiring a roll to DP1.2a PHY CTS.
  - Both DP 1.2a Specification and DP1.2a PHY Specification will be released soon.

What Changes in **1.2a DP Spec**?

- **HBR2** TP3_EQ Definitions
  - DP1.2 – 2 Equalizers
    - Source & Sink



- DP 1.2a - Single Equalizer for both



$$H(s) = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2}\cdot\sqrt{\omega^2+\omega_{p2}^2}\cdot\sqrt{\omega^2+\omega_{p3}^2}}$$

where

$\omega_z = 2\pi(0.45\times10^9)$

$\omega_{p1} = 2\pi(2.7\times10^9)$

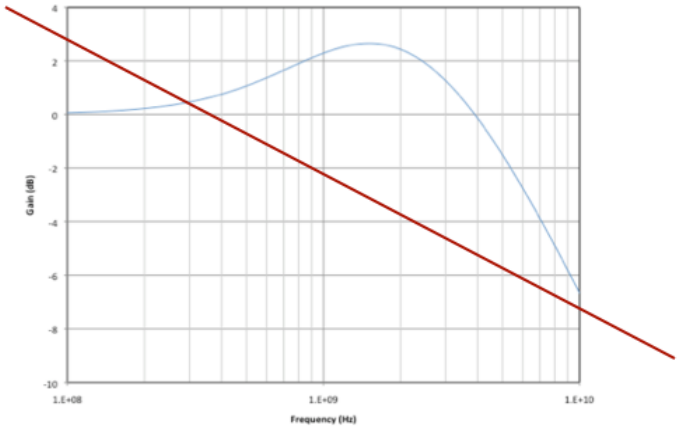
$\omega_{p2} = 2\pi(4.5\times10^9)$

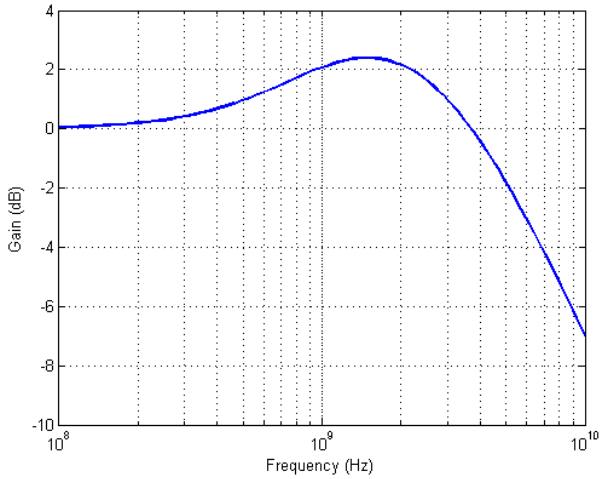
$\omega_{p3} = 2\pi(13.5\times10^9)$

$\omega_z = 0.64 \times 10^6$

What Changes in **1.2a DP Spec**?

- **HBR** Equalizer Definition





$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2} \cdot \sqrt{\omega^2+\omega_{p2}^2}}$$

where

$$\omega_z = 2\pi(0.7\times10^9)$$

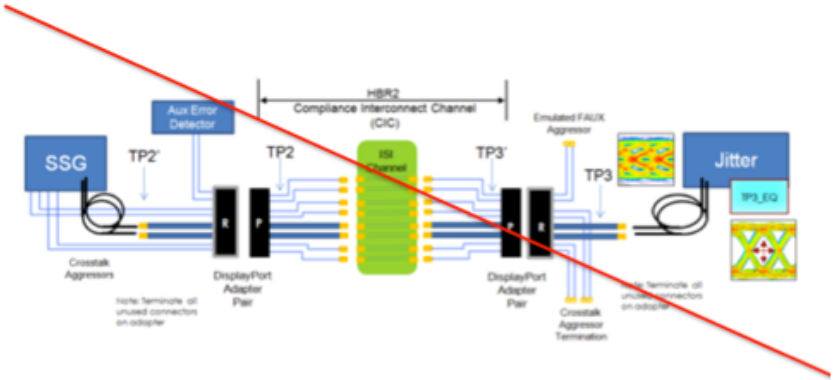
$$\omega_{p1} = 2\pi(1.35\times10^9)$$

$$\omega_{p2} = 2\pi(2.5\times10^9)$$

$\omega_z = 0.725 \times 10^6$

What Changes in **1.2a DP PHY CTS**?

- Reference to new TP3_Eq Equalizer values in DP 1.2a Specification
- Eye Height for sources reduced from 120mV to 90mV
  - Same value as Sink Stressed Eye Calibration
- Addition of TP1-TP2 ISI
  - Required to achieve proper ISI at TP3_Eq
- Addition of DP++ (Dual Mode) Eye and Jitter Tests
  - Omission from the DP1.2 Version



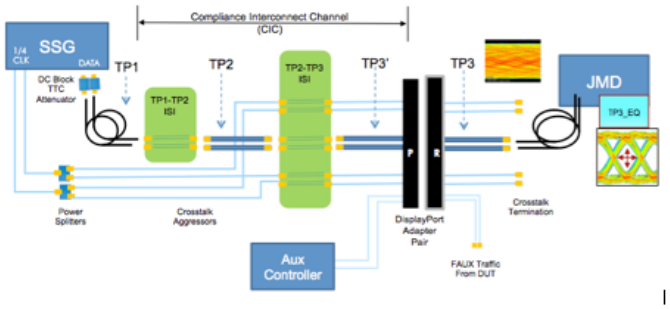
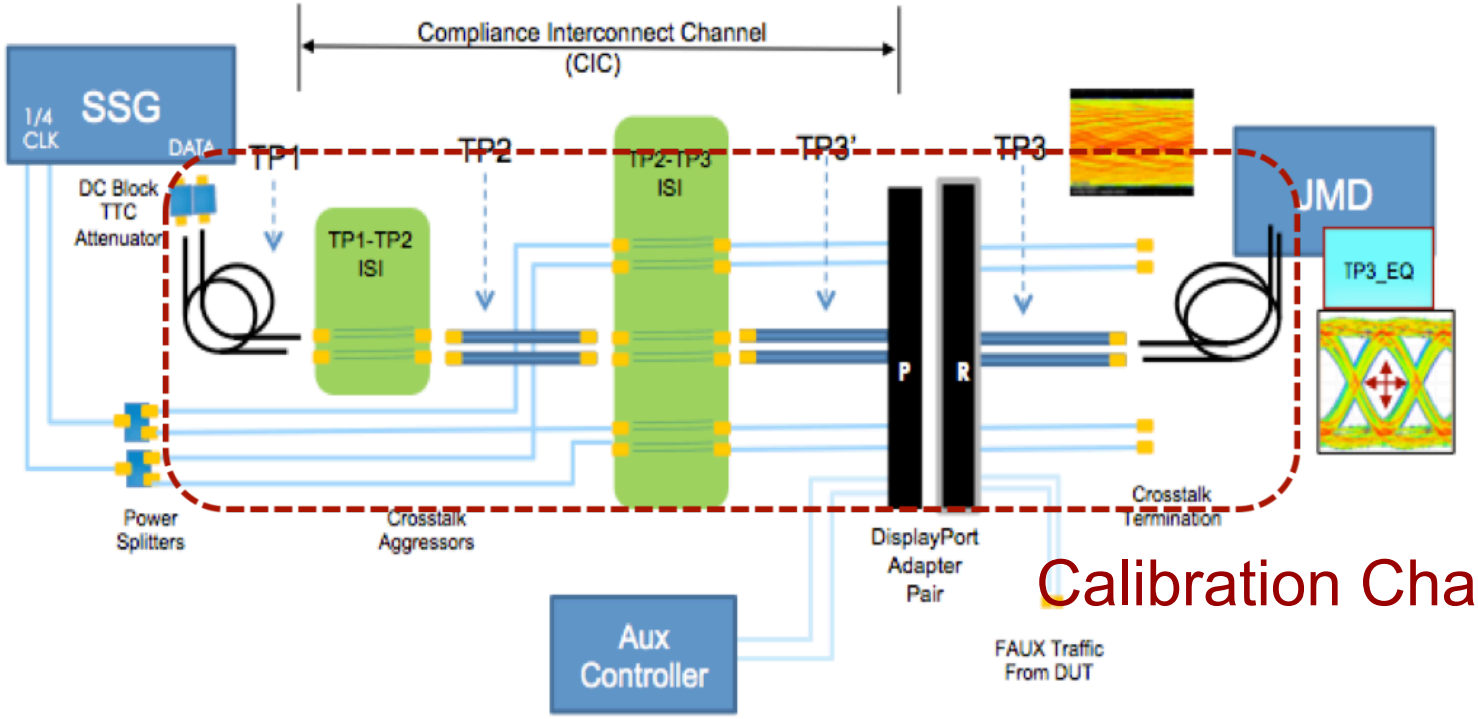


Figure 4-3: HBR and HBR2 Jitter Tolerance Testing Calibration Setup

HBR/HBR2 Sink Calibration



Calibration Challenge!

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Calibration Challenge

- ISI at TP3-Eq is a Function of:
  - BERT Rise Time
  - ISI Channel Used
  - Cables and Connectors Used
  - Equalizer Frequency Response

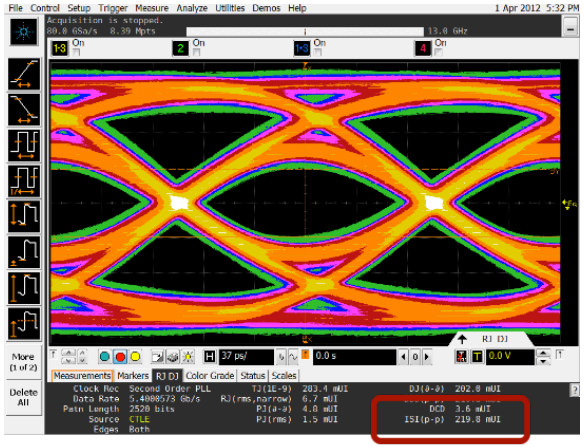

Table 4-4: Jitter Component Settings for High Bit Rate 2

f(SJ) [MHz]	TJ(JTHBR2rx) [mUI]	ISI [mUI]	RJ(RMS) [mUI]	Approximate SJ_{SWEEP} [mUI]	SJ_{FIXED} @ 200MHz [mUI]
2	1026	220	16.7	505	100
10	636	220	16.7	116	100
20	624	220	16.7	104	100
100	620	220	16.7	100	100

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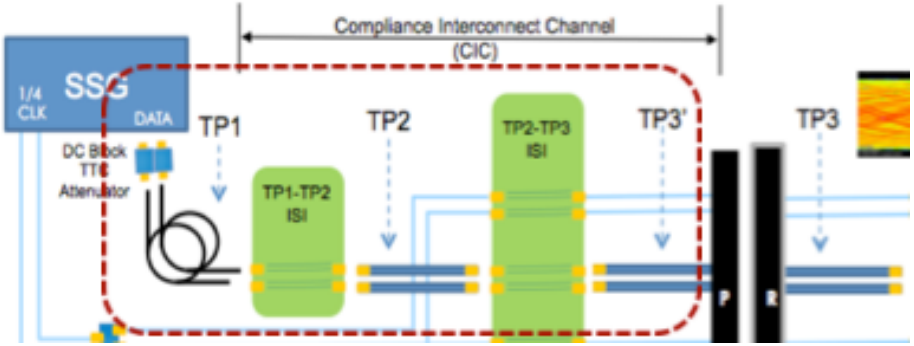
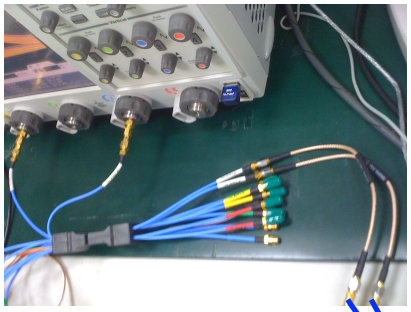
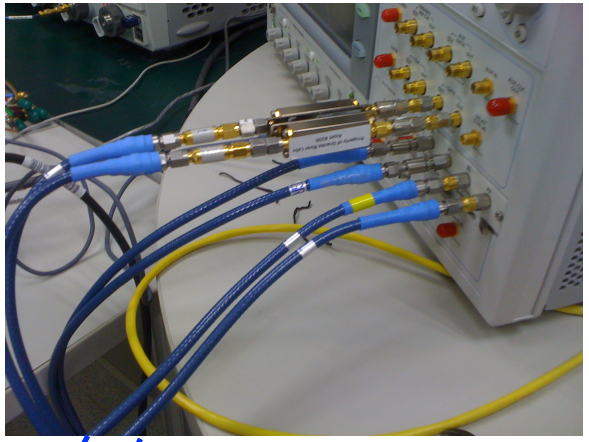
Method of Implementation

- Combine two ISI Channels into one.
- Example: JBERT with Opt. J20
  - 100ps TTCs
  - 6dB Attenuation
  - DC Block
  - 1 Meter SMA Cables
  - 28" ISI Channel (Opt. J20)
  - 1 Meter SMA Cables
  - Short SMA Cable/Connector for Calibration
  - Wilder DP Mated Pair Adapter







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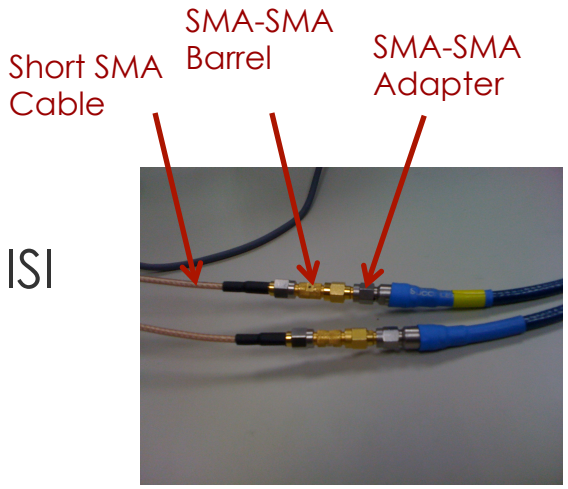
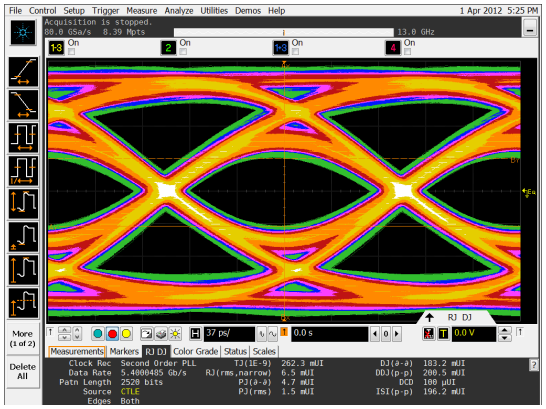
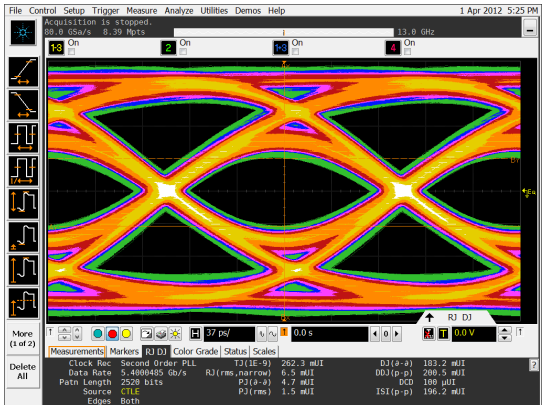
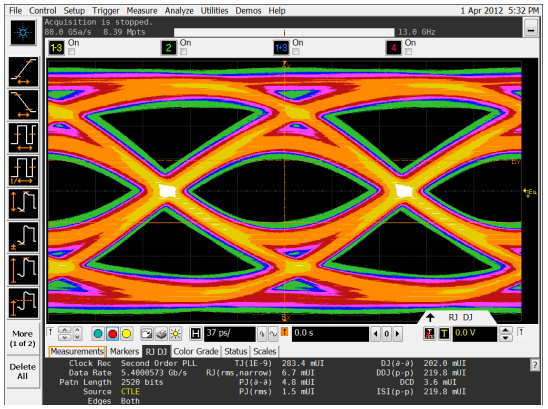
Cables/Connectors for TP3_Eq ISI Calibration

- No Short Cable = 196 mUI ISI
- Short Cable + SMA Barrel = 207 mUI ISI
- SMA-SMA Adapter = 219.8 mUI









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To Get HBR TP3_Eq ISI

- Replace 100ps TTC with 150ps TTC
- Reduce ISI Channel to 20”

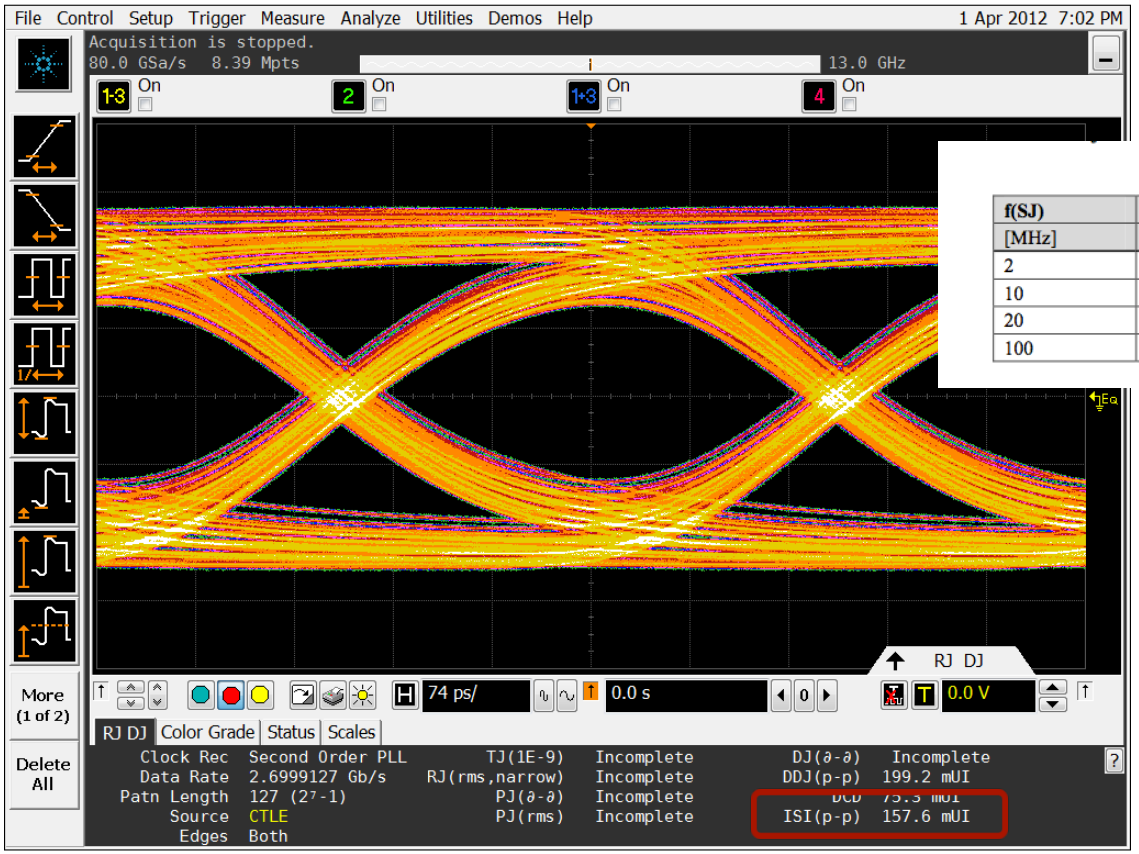


Table 4-3: Jitter Component Settings for High Bit Rate

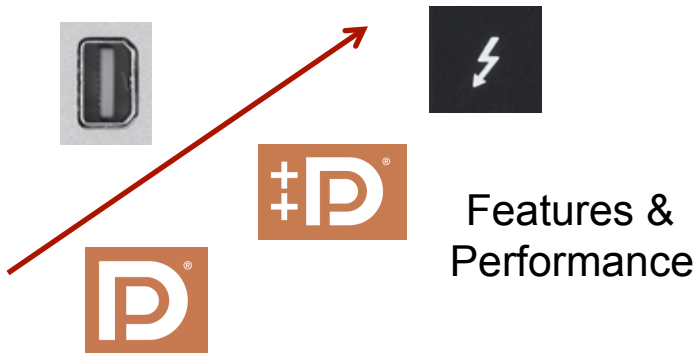
f(SJ) [MHz]	TJ(JTHBRrx) [mUI]	ISI [mUI]	RJ(RMS) [mUI]	Approximate SJ [mUI]
2	1227	161	13.5	904
10	548	161	13.5	225
20	505	161	13.5	182
100	491	161	13.5	168

Recommended ATC and TE Vendor Requirements

- Document TP3_Eq ISI Calibration Measurement for HBR2 and HBR as part of Data Set
  - Eye Diagram and ISI Measurement
- Measure ISI at TP3_Eq to Target Value +/- 5% of Specification
  - 5% Tolerance to allow small differences in physical setup
- Next Step is to rationalize Crosstalk with single ISI channel.

What about DP in Thunderbolt?

- Does TBT Compliant mean DP Compliant?
  - Section 3 of DP PHY CTS - DP Source (HBR/RBR)
  - Section 7 of the HDMI 1.4 CTS – HDMI Source Testing
    - Test DP++ electrical signals through a DP a compliant Dual Mode adapter
  - Functional test spec takes the place of the DP Interop Spec.
  - Link Layer has been Certified DP Compliant at the chip level
    - GRL Certified
- One mini-DP connector – Can have 3 possible logos!



Summary

- Current version of the **DP Specification is DP1.2**
- Compliance test program is in transition between 1.1a and 1.2(a)
- The difference between 1.2 and 1.2a **DP Specification** is the definition of the equalizer for TP3_Eq
  - Resulting in changes in the **DP PHY CTS** from 1.2 to 1.2a
- DP (HBR/RBR) is a subset of Thunderbolt Testing and uses the same mDP connector and is being tested to the DP 1.2 logo requirements

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