iDP™ (Internal DisplayPort™) Technology Overview

New Generation Large-Screen Display Internal Interface

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- Why iDP
- iDP PHY Layer
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- Comparison between Constant and Variable Link Rate
DisplayPort Family

- **DP (DisplayPort)**
  - Connection to TV, Monitors from an external source

- **eDP (embedded DP)**
  - Connection between GFx and notebook panel

- **iDP (internal DP)**
  - Connection between Display controller and TCON within a large-screen display (e.g., DTV display)

![Diagram showing DP, eDP, and iDP connections](image-url)
# DisplayPort Family (as of DEC 2010)

<table>
<thead>
<tr>
<th></th>
<th>DP1.2</th>
<th>eDP</th>
<th>iDP</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Standard</strong></td>
<td>VESA V1.2 Jan 2010</td>
<td>VESA V1.2: May 2010</td>
<td>VESA : iDP1.0 Released Apr 2010</td>
</tr>
<tr>
<td><strong>PHY</strong></td>
<td></td>
<td></td>
<td>AC Coupled / CDR / ANSI 8b/10b</td>
</tr>
<tr>
<td><strong>Bandwidth (per lane)</strong></td>
<td>HBR 5.4Gbps</td>
<td></td>
<td>Nominal 3.24Gbps/lane</td>
</tr>
<tr>
<td></td>
<td>HBR 2.7Gbps</td>
<td></td>
<td>Other link rates: Implementation Choice (e.g., 3.78Gbps/lane)</td>
</tr>
<tr>
<td></td>
<td>RBR 1.62Gbps</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Lane Count</strong></td>
<td>1, 2, or 4 lanes</td>
<td>1, 2, or 4 lanes</td>
<td>1 ~ 16 lanes per bank</td>
</tr>
<tr>
<td><strong>Secondary Data Packet</strong></td>
<td>YES</td>
<td>Optional</td>
<td>NO</td>
</tr>
<tr>
<td><strong>AUX CH</strong></td>
<td>YES (incl.vUSB2.0 transport over AUX)</td>
<td>Optional (used for backlight/color control)</td>
<td>NO</td>
</tr>
<tr>
<td><strong>HPD</strong></td>
<td>YES</td>
<td>Optional</td>
<td>YES (Used for Link Training Pattern transmission trigger)</td>
</tr>
<tr>
<td><strong>Transported data</strong></td>
<td>Multiple A/V streams</td>
<td>Video Stream</td>
<td>Video Stream</td>
</tr>
<tr>
<td></td>
<td>Control data</td>
<td>Control data</td>
<td></td>
</tr>
<tr>
<td><strong>Stream Clocking Mode</strong></td>
<td>Synchronous or Asynchronous to Link Symbol Clock</td>
<td>Synchronous only; Nvid fixed to 48 decimal</td>
<td></td>
</tr>
<tr>
<td><strong>Target Application</strong></td>
<td>Box2Box connection to TV/Monitor with Multi-stream</td>
<td>Internal to Notebook/Netbook/Notepad/All-in-one PC</td>
<td>Internal to TV/monitor chassis</td>
</tr>
</tbody>
</table>

**VESA**

V1.2: Jan 2010

**DisplayPort**

V1.2: May 2010

**iDP**

VESA : iDP1.0 Released Apr 2010

**PHY**

HBR 5.4Gbps, HBR 2.7Gbps, RBR 1.62Gbps

**LANE COUNT**

1, 2, or 4 lanes

**SECONDARY DATA PACKET**

YES, Optional

**AUX CH**

YES (incl. vUSB2.0 transport over AUX), Optional (used for backlight/color control)

**HPD**

YES, Optional

**TRANSPORTED DATA**

Multiple A/V streams, Control data

**STREAM CLOCKING MODE**

Synchronous or Asynchronous to Link Symbol Clock

**TARGET APPLICATION**

Box2Box connection to TV/Monitor with Multi-stream, Internal to Notebook/Netbook/Notepad/All-in-one PC

**VESA**

V1.2: May 2010

**DisplayPort**

V1.2: May 2010

**iDP**

VESA : iDP1.0 Released Apr 2010
iDP Compliance Test Guideline Document

- Companion guideline document to iDP Standard Specification V1.0
- Describes compliance test methods for a source device, a sink device, and a cable/connector assembly
  - Covers PHY and Link Layer compliance testing
  - Applicable to 3.24Gbps/lane and other link rates such as 3.78Gbps/lane
  - Lists reference connector pin-outs
    - 41 pin for 4 lanes (also used for a test fixture)
    - 51 pin for 8 lanes
- Expected to be published in DEC 2010 ~ JAN 2011
Why iDP?

- Ever increasing TV applications demand for bandwidth

<table>
<thead>
<tr>
<th>Year</th>
<th>Technology Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>2008</td>
<td>FHD 60Hz, 4.5Gb/s</td>
</tr>
<tr>
<td></td>
<td>9Gb/s, 120Hz</td>
</tr>
<tr>
<td></td>
<td>18Gb/s</td>
</tr>
<tr>
<td>2012</td>
<td>FHD 240Hz</td>
</tr>
<tr>
<td></td>
<td>18Gb/s</td>
</tr>
<tr>
<td></td>
<td>UD (4k x 2k)/120Hz</td>
</tr>
<tr>
<td></td>
<td>36Gb</td>
</tr>
</tbody>
</table>

- Use of LVDS is becoming un-manageable
  - Signal integrity issues
  - Poor EMI performance
  - Too many connectors, wires, pins on TV SoC and T-CON
  - Cost
iDP Benefits

- Proven Technology in a various of applications
  - Most reliable and robust link based on proven DP technology

- Open and Royalty- Free Industry Standard

- International VESA Standard
  - VESA members free in contribution in Spec. / IP development

- Far fewer number of wires than LVDS

- Much lower EMI than LVDS

- Constant link rate for the utmost link stability
iDP vs. LVDS: Signal Count Comparison

- **LVDS**

<table>
<thead>
<tr>
<th>LVDS</th>
<th>FHD(10bit)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>60Hz</td>
</tr>
<tr>
<td>No. of signals</td>
<td>24</td>
</tr>
</tbody>
</table>

- **iDP: Based on nominal 3.24 Gbps/lane (Main Link plus HPD)**

<table>
<thead>
<tr>
<th>iDP</th>
<th>FHD(10bit)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>60Hz</td>
</tr>
<tr>
<td>No. of signals</td>
<td>5</td>
</tr>
</tbody>
</table>
iDP vs. LVDS: EMI Data

Identical setup for iDP & LVDS
- 1.0 meter FFC
- STM TX and RX Board
- 5 Volts -AC Adaptor
- Video Pattern: Blue/Grey Bar

EMI Peaks
- LVDS: from LVDS CLK=74.28MHz
- Red Circles: from System Ref.CLK

15dB~25dB Improvement

1) With switching regulator in board
2) Blue Circles (LVDS) : EMI peaks from Pixel Clock and also from system clock
3) Red Circles (iDP): Only EMI from system clock
iDP PHY Layer
1) Now LVDS IF is transitioning to eDP. 2) Until USB 2.0: based on a half-duplex differential signaling. 3) Apple / Lenovo / HP / Dell shipping MAC/PC with DP output for the external monitor interface.
iDP PHY Electrical Sub-Layer

iDP PHY Layer taken from a **proven DisplayPort** design

![Diagram of iDP PHY Layer](image)

- **iDP PHY Layer**
  - Source Device
  - Sink Device
  - ANSI 8B/10B
  - GAIN/Pre-EM
  - EQ (Optional)
  - CDR

- **iDP PHY Layer a subset of DP1.2**
Pre-Emphasis by iDPTX (Mandatory)

At high bit rates and/or over long distance, the signal degrades

Transmitter [Source]  Low Frequency or long bit

Receiver [Sink]  High Frequency or short bit

Pre-emphasis helps facilitate clock recovery and symbol lock by a sink device via compensating for frequency-dependent insertion loss of channel

Transmitter [Source]  Receiver [Sink]

Higher Voltage Swing on short bit [over long distance]
Channel Equalization by iDPRX (Optional)
iDP PHY Logical Sub-Layer

- **Link Training**
  - iDPRX prompts iDPTX to transmit link training pattern by generating a low-going pulse

- **Inter-lane skew**
  - Two link symbols between adjacent lanes

  \[
  LaneSkew = 2 \times LS\!Clk \text{ cycles} \times \left[ \text{Remainder of} \left( \frac{\text{LaneCount}}{4} \right) \right]
  \]

- **Data symbol scrambling**
  - Seed value = FFFEh; same as eDP, different from DP

- **ANSI8B/10B channel coding**
iDP Link Layer
# iDP Link Layer

iDP Link Layer is a subset of the DP Standard: Far lighter

<table>
<thead>
<tr>
<th>iDP Link Layer</th>
<th>Descriptions</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDP</td>
<td>None</td>
</tr>
<tr>
<td>AUX</td>
<td>None</td>
</tr>
<tr>
<td>Content Protection</td>
<td>None</td>
</tr>
<tr>
<td>Clocking Mode</td>
<td>Synchronous Nvid =48 dec and Mvid = 8 bits</td>
</tr>
<tr>
<td>MSA Packet</td>
<td>Only MISC0 and MISC1 bit7 and bit2:1 and H width and V height</td>
</tr>
</tbody>
</table>
Data Rate Throttling

- iDPTX, upon receiving pixel data from a stream source, throttles the pixel data rate
- Supports various pixel rates over constant-rate link with Nvid value fixed to 48 decimal
- Dependent on the buffer size in iDPTX, realizes horizontal blanking reduction transparently to a stream source and an iDPRX TCON

<table>
<thead>
<tr>
<th></th>
<th>Standard Video</th>
<th>HBLANK</th>
<th>Standard iDP Video</th>
<th>Throttled iDP Video</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Active Video Period</td>
<td>HBLANK</td>
<td>Active Video Period</td>
<td>Active Video Period</td>
</tr>
<tr>
<td>Standard iDP Video</td>
<td>Active Video Period (TU’s)</td>
<td>Sea of Dummy symbols</td>
<td>Active Video Period (TU’s)</td>
<td>Active Video Period (TU’s)</td>
</tr>
<tr>
<td>Throttled iDP Video</td>
<td>Active Video Period (TU’s)</td>
<td>Sea of Dummy symbols</td>
<td>Active Video Period (TU’s)</td>
<td>Active Video Period (TU’s)</td>
</tr>
</tbody>
</table>
3D Supporting in iDP Standard

iDP1.0 supports inband signaling for stereoscopic 3D transport

<table>
<thead>
<tr>
<th>Bits</th>
<th>Bit7</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>“Don’t care”</td>
<td>No 3D Stereo video being transported</td>
</tr>
<tr>
<td>01</td>
<td>“Don’t care”</td>
<td>Frame sequential 3D Stereo video transported and the next (upcoming) frame is Right EYE frame</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td>Line interleaved 3D Stereo video transported, lines 1, 3, 5, … carry Right EYE frame, and lines 2, 4, 6, … carry Left EYE frame, and lines 1, 3, 5, … carry Right EYE frame, and lines 2, 4, 6, … carry Left EYE frame</td>
</tr>
<tr>
<td>11</td>
<td>“Don’t care”</td>
<td>Frame sequential 3D Stereo video transported and the next (upcoming) frame is Left EYE frame</td>
</tr>
</tbody>
</table>

Note: When 3D Stereo video is transported in a frame sequential manner, MISC1 Bits 2:1 toggle between 01 and 11 frame by frame.

How Left EYE and Right EYE data are transported with frame sequential and line-interleaved transport methods is shown in Figure 2-3.

- Miscellaneous (MISC1, 8 bits)
  - Interlaced vertical total even (bit 0)
    - 0 = Number of lines per interlaced frame (consisting of two fields) is an odd number
    - 1 = Number of lines per interlaced frame (consisting of two fields) is an even number
  - Stereo video attribute (bits 2:1)
    - 00 = No stereo video transported
    - 01
      - For progressive video, the next frame is RIGHT eye
      - For interlaced video, TOP field is RIGHT eye and BOTTOM field is LEFT eye
    - 10 = RESERVED and must not be used
    - 11
      - For progressive video, the next frame is LEFT eye
      - For interlaced video, TOP field is LEFT eye and BOTTOM field is RIGHT eye

Figure 2.32: Field Sequential Stereo Format with Left View and Right View Indicated via MISC1 Bits 2:1 of the MSA Packet
Comparison between Constant Link Rate and Variable Link Rate
PHY Comparison between Constant and Variable Link Rate

**Constant Link Rates [iDP]**

- **Nominal 3.24 Gbps Link Rate Or Higher**
- Link Rate = \( Q \times \text{Ref.Clk} = 3.24 \text{ Gbps or higher} \)
- \( \text{Ref.Clk from low jitter crystal} \)

**Variable Link Rate from Pixel Clock**

- **Variable Link Rate**
- \( \text{LS CLK} = N \times \text{Input Pixel Clk} \)
- Input Pixel Clock bound to be jittery

<table>
<thead>
<tr>
<th></th>
<th>Constant Link Rate (iDP)</th>
<th>Variable Link Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Architectural Concept</strong></td>
<td><strong>From the optimized High Speed Signaling</strong></td>
<td><strong>From Legacy Video Interface</strong></td>
</tr>
<tr>
<td><strong>Link Rates</strong></td>
<td><strong>Pixel Clock Decoupled</strong></td>
<td><strong>Pixel Clock Coupled tightly</strong></td>
</tr>
<tr>
<td><strong>Link Stability</strong></td>
<td><strong>Steady and Uninterruptible</strong></td>
<td><strong>Unstable and interruptible by Pixel Clock Variation/Change</strong></td>
</tr>
</tbody>
</table>
PHY Comparison between Constant and Variable Link Rate

- **Constant Link Rate (iDP):** Link Symbol Clock generated from a stable, jitter-free reference clock (e.g., crystal oscillator)
- **Variable Link Rate:** Link Symbol Clock generated using pixel clock as a reference clock

**Signal Integrity:** Constant (iDP) >= Variable Link Rate
- At High Speed Signaling, the lowest jitter clock is a key technology to make a bigger eye-opening at the same conditions.

Every proven high speed signaling is using constant link rate.

- DP1.1a/1.2
- PCI Express
- USB 3.0
- SATA

Allow to use the less jittery reference clock.
Constant Link Rate (iDP): Link Symbol Clock generated from a stable, jitter-free reference clock (e.g., crystal oscillator)
Variable Link Rate: Link Symbol Clock generated using pixel clock as a reference clock

**Maximum Link Rate**: Constant (iDP) >= Variable Link Rate

The jitter of reference clock defines the maximum link rate at high speed signaling, an Constant link rate can use less jittery reference clock at any scenario.

Constant Link Rate (iDP) can support higher link rates at any scenario compared to a variable link rate (from a pixel clock).

- DP1.2 = 5.4Gbps
- USB 3.0 = 5Gbps
- SATA = 6Gbps

Only iDP based on a proven technology.
PHY Comparison between Constant and Variable Link Rate

- **Constant Link Rate (iDP):** Link Symbol Clock generated from a stable, jitter-free reference clock (e.g., crystal oscillator)
- **Variable Link Rate:** Link Symbol Clock generated using pixel clock as a reference clock

**Link Stability during video format change:** Constant (iDP) >> Variable Link Rate

Pixel CLK is bound to change at any time in ATSC/DVB Application. Especially problematic for MEMC based 120-/240-Hz frame rate conversion algorithm implementation. With a variable link rate, the display should be turned off during channel / mode / input changes and it requires new Clock Recovery/Symbol Lock Sequence, if any pixel clock changes.

Only iDP (Constant Link Rate) can allow a seamless transition during channel/mode/input changes including pixel frequency variations.
THANK YOU