

iDP™ (Internal DisplayPort™) Technology Overview

New Generation Large-Screen Display Internal Interface

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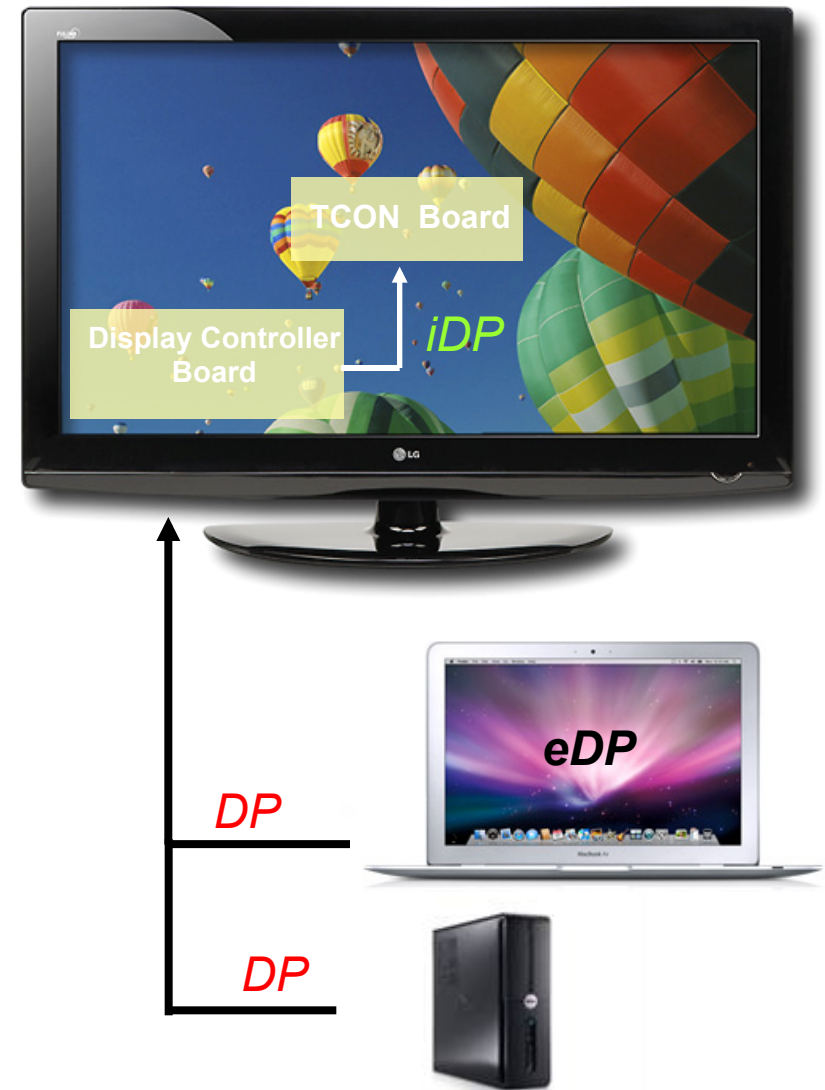


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- Display Port Family
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- iDP PHY Layer
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- Comparison between Constant and Variable Link Rate

DisplayPort Family

- **DP (DisplayPort)**
 - Connection to TV, Monitors from an external source
- **eDP (embedded DP)**
 - Connection between GFX and notebook panel
- **iDP (internal DP)**
 - Connection between Display controller and TCON within a large-screen display (e.g., DTV display)



DisplayPort Family (as of DEC 2010)

	DP1.2	eDP	iDP
Standard	VESA V1.2 Jan 2010	VESA V1.2: May 2010	VESA : iDP1.0 Released Apr 2010
PHY	AC Coupled / CDR / ANSI 8b/10b		
Bandwidth (per lane)	HBR2 5.4Gbps HBR 2.7Gbps RBR 1.62Gbps	HBR 2.7Gbps RBR 1.62Gbps	Nominal 3.24Gbps/lane Other link rates: Implementation Choice (e.g., 3.78Gbps/lane)
Lane Count	1, 2, or 4 lanes	1, 2, or 4 lanes	1 ~ 16 lanes per bank
Secondary Data Packet	YES	Optional	NO
AUX CH	YES (incl.vUSB2.0 transport over AUX)	Optional (used for backlight/ color control)	NO
HPD	YES	Optional	YES (Used for Link Training Pattern transmission trigger)
Transported data	Multiple A/V streams Control data	Video Stream Control data	Video Stream
Stream Clocking Mode	Synchronous or Asynchronous to Link Symbol Clock		Synchronous only; Nvid fixed to 48 decimal
Target Application	Box2Box connection to TV/Monitor with Multi-stream	Internal to Notebook/ Netbook /Notepad/All-in-one PC	Internal to TV/monitor chassis

iDP Compliance Test Guideline Document

- Companion guideline document to iDP Standard Specification V1.0
- Describes compliance test methods for a source device, a sink device, and a cable/connector assembly
 - Covers PHY and Link Layer compliance testing
 - Applicable to 3.24Gbps/lane and other link rates such as 3.78Gbps/lane
- Lists reference connector pin-outs
 - 41 pin for 4 lanes (also used for a test fixture)
 - 51 pin for 8 lanes
- Expected to be published in DEC 2010 ~ JAN 2011

Why iDP ?

- Ever increasing TV applications demand for bandwidth



- Use of LVDS is becoming un-manageable
 - Signal integrity issues
 - Poor EMI performance
 - Too many connectors, wires, pins on TV SoC and T-CON
 - Cost

iDP Benefits

- Proven Technology in a various of applications
 - Most reliable and robust link based on proven DP technology
- Open and Royalty- Free Industry Standard
- International VESA Standard
 - VESA members free in contribution in Spec. / IP development
- Far fewer number of wires than LVDS
- Much lower EMI than LVDS
- Constant link rate for the utmost link stability

iDP vs. LVDS: Signal Count Comparison

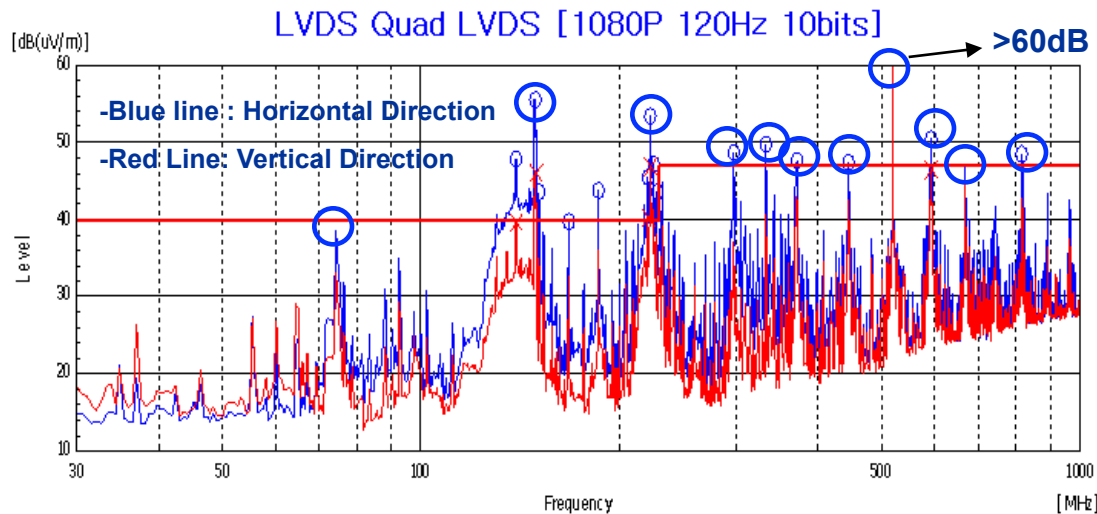
➤ LVDS

LVDS	FHD(10bit)		
	60Hz	120Hz	240Hz
No. of signals	24	48	96

➤ iDP: Based on nominal 3.24 Gbps/lane (Main Link plus HPD)

iDP	FHD(10bit)		
	60Hz	120Hz	240Hz
No. of signals	5	9	17

iDP vs. LVDS: EMI Data

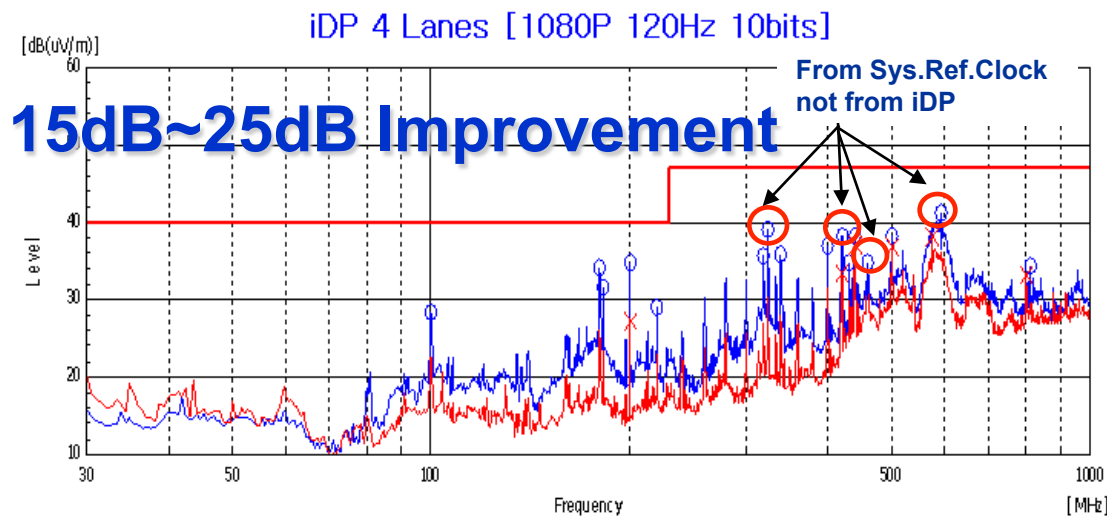


Identical setup for iDP & LVDS

- 1.0 meter FFC
- STM TX and RX Board
- 5 Volts -AC Adaptor ¹⁾
- Video Pattern: Blue/Grey Bar

EMI Peaks

- LVDS: from LVDS CLK=74.28MHz ²⁾
- Red Circles: from System Ref.CLK ³⁾



- 1) With switching regulator in board
- 2) Blue Circles (LVDS) : EMI peaks from Pixel Clock and also from system clock
- 3) Red Circles (iDP): Only EMI from system clock

iDP PHY Layer

CDR with ANSI 8B/10B Channel Coding

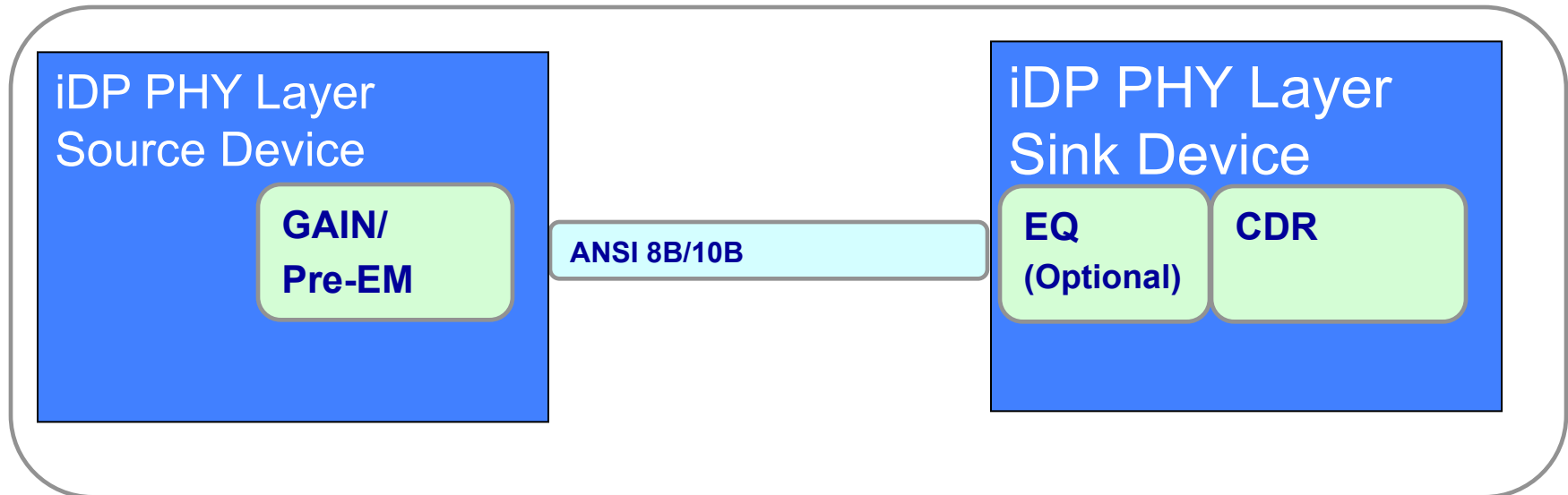
iDP Technology based on CDR with ANSI8B/10B, proven in data communication industry.



1) Now LVDS IF is transitioning to eDP. 2)Until USB 2.0:based on a half-duplex differential signaling
3) Apple /Lenovo /HP/Dell shipping MAC/PC with DP output for the external monitor interface

iDP PHY Electrical Sub-Layer

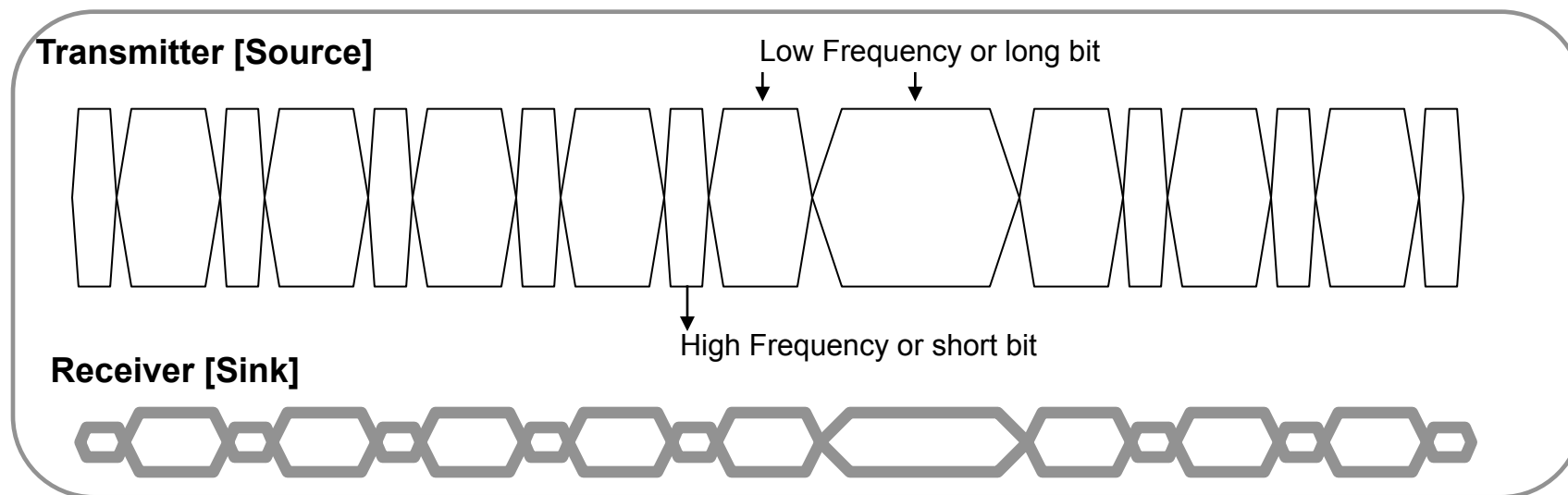
iDP PHY Layer taken from a **proven DisplayPort** design



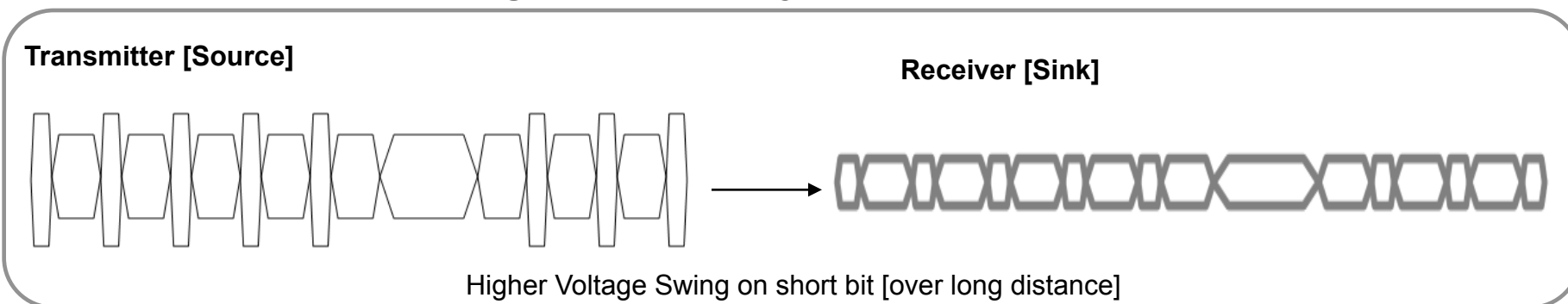
◆ iDP PHY Layer a subset of DP1.2

Pre-Emphasis by iDPTX (Mandatory)

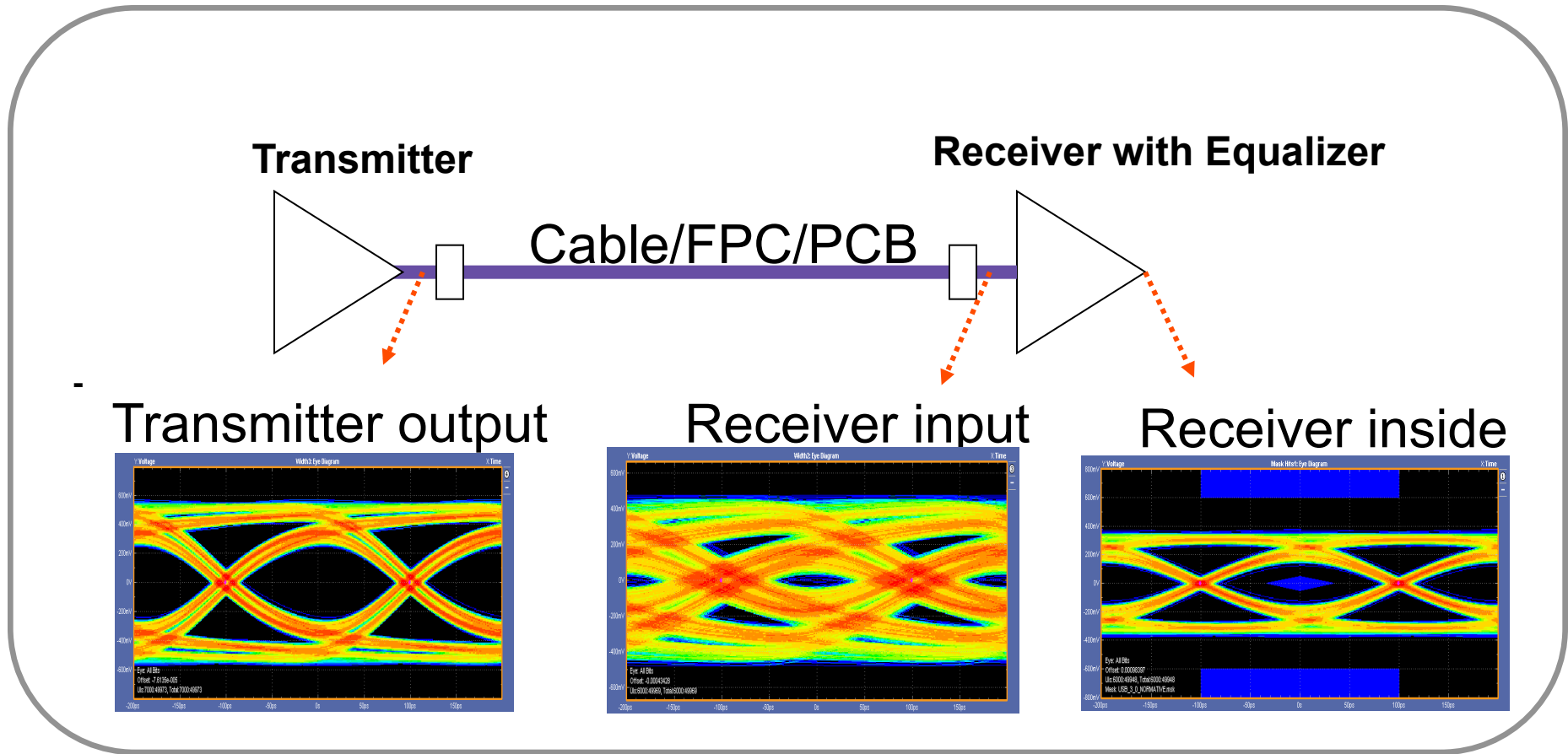
At high bit rates and/or over long distance, the signal degrades



Pre-emphasis helps facilitate clock recovery and symbol lock by a sink device via compensating for frequency-dependent insertion loss of channel



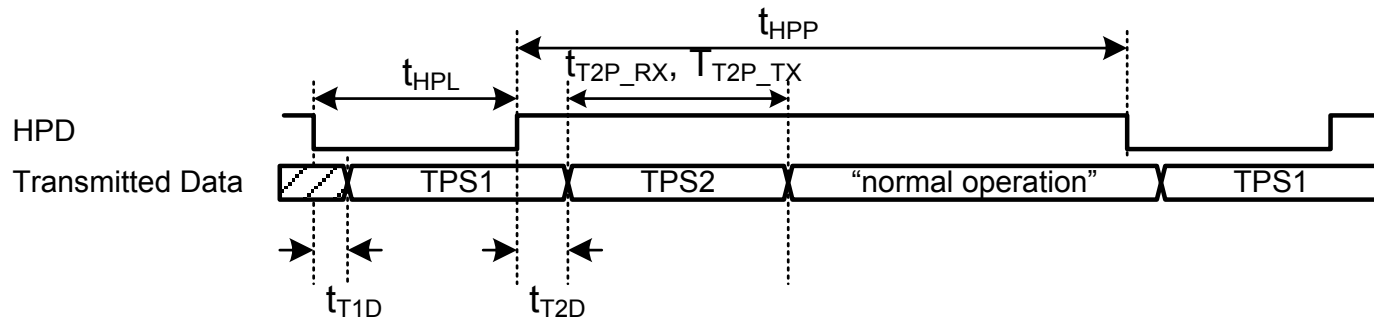
Channel Equalization by iDPRX (Optional)



iDP PHY Logical Sub-Layer

➤ Link Training

- iDPRX prompts iDPTX to transmit link training pattern by generating a low-going pulse



➤ Inter-lane skew

- Two link symbols between adjacent lanes

$$LaneSkew = 2 * LSClk \text{ cycles} * \left[\text{Remainder of } \left(\frac{LaneCount}{4} \right) \right]$$

➤ Data symbol scrambling

- Seed value = FFFEh; same as eDP, different from DP

➤ ANSI8B/10B channel coding



iDP Link Layer

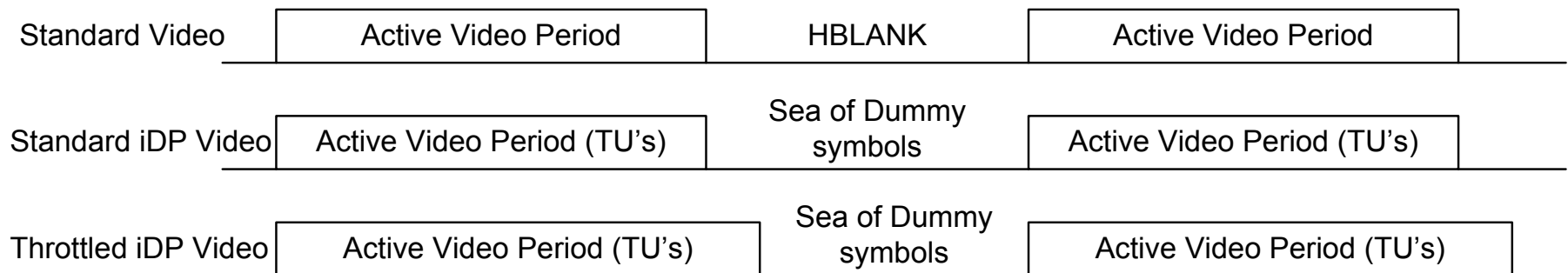
iDP Link Layer

iDP Link Layer is a subset of the DP Standard: Far lighter

	iDP Link Layer	Descriptions
SDP	None	Enabling the simplest Link Design
AUX	None	Enabling the simplest Link Design
Content Protection	None	Enabling the simplest Link Design
Clocking Mode	Synchronous Nvid =48 dec and Mvid = 8 bits	Allowing the smallest pixel clock regeneration PLL
MSA Packet	Only MISC0 and MISC1 bit7 and bit2:1 and H width and V height	Simplified, but supporting in-band signaling for stereoscopic 3D transport

Data Rate Throttling

- iDPTX, upon receiving pixel data from a stream source, throttles the pixel data rate
 - Supports various pixel rates over constant-rate link with Nvid value fixed to 48 decimal
 - Dependent on the buffer size in iDPTX, realizes horizontal blanking reduction transparently to a stream source and an iDPRX TCON



3D Supporting in iDP Standard

iDP1.0 supports inband signaling for stereoscopic 3D transport

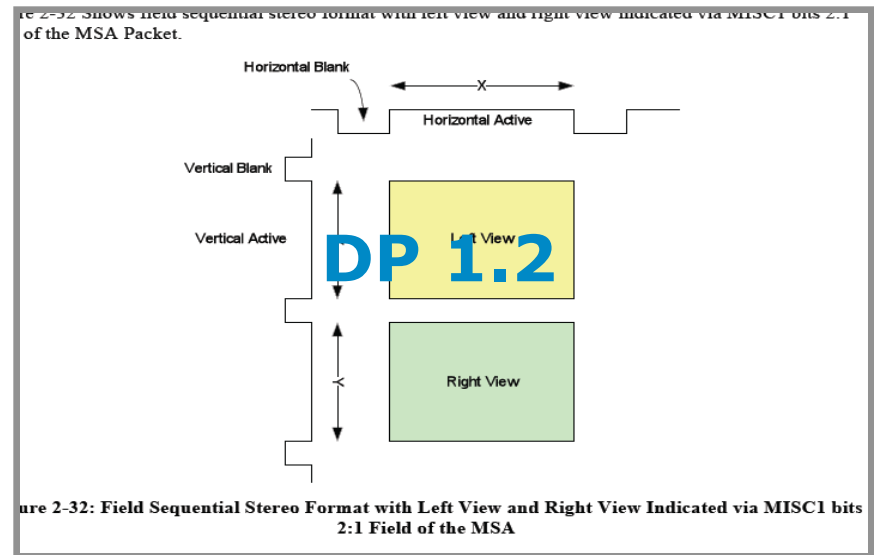
Table 2-2: MISC1 Bit Definition for 3D Stereo Video Transport Indication

Bits2:1	Bit7	Definition
00	“Don’t care”	No 3D Stereo video being transported
01 ¹	“Don’t care”	Frame sequential 3D Stereo video transported and the next (upcoming) frame is Right EYE frame
10	0	Line interleaved 3D Stereo video transported; lines 1, 3, 5, ... carry Left EYE frame, and lines 2, 4, 6, ... carry Right EYE frame, and
10	1	Line interleaved 3D Stereo video transported; lines 1, 3, 5, ... carry Right EYE frame, and lines 2, 4, 6, ... carry Left EYE frame, and
11 ¹	“Don’t care”	Frame sequential 3D Stereo video transported and the next (upcoming) frame is Left EYE frame

Note¹: When 3D Stereo video is transported in a frame sequential manner, MISC1 Bits2:1 toggle between 01 and 11 frame by frame.

How Left EYE and Right EYE data are transported with frame sequential and line-interleaved transport methods is shown in Figure 2-5.

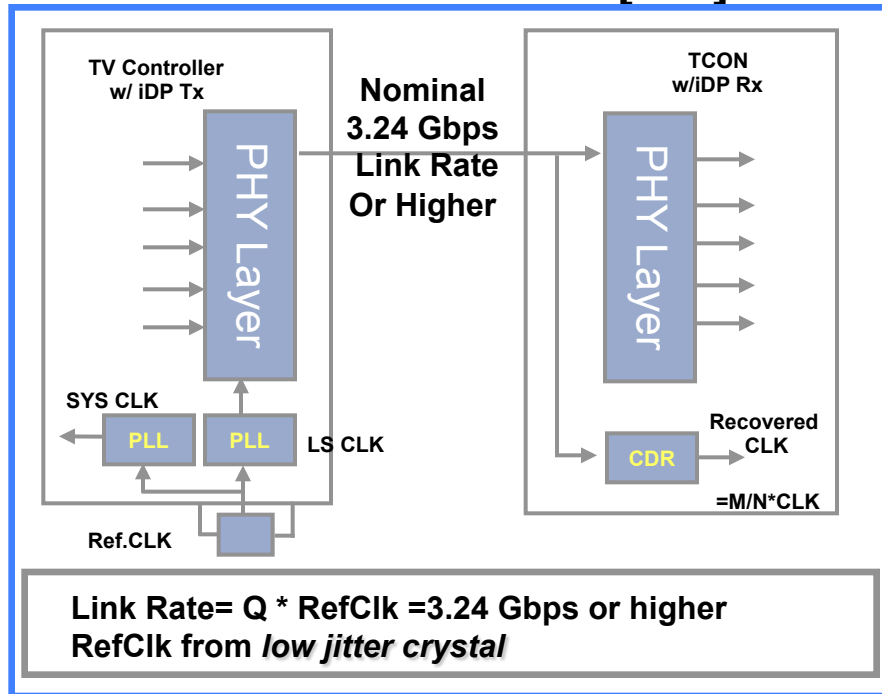
- Miscellaneous1 (MISC1, 8 bits)
 - Interlaced vertical total even (bit 0)
 - 0 = Number of lines per interlaced frame (consisting of two fields) is an odd number.
 - 1 = Number of lines per interlaced frame (consisting of two fields) is an even number.
 - Stereo video attribute (bits 2:1)
 - 00 = No stereo video transported
 - 01
 - For progressive video, the next frame is RIGHT eye
 - For interlaced video, TOP field is RIGHT eye and BOTTOM field is LEFT eye
 - 10 = RESERVED and must not be used
 - 11
 - For progressive video, the next frame is LEFT eye
 - For interlaced video, TOP field is LEFT eye and BOTTOM field is RIGHT eye



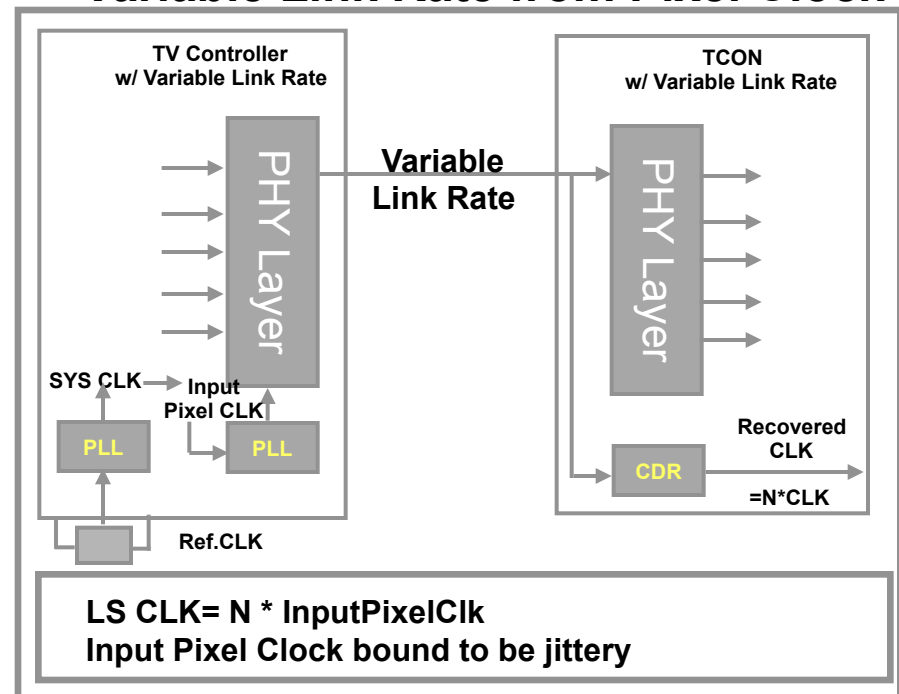
Comparison between Constant Link Rate and Variable Link Rate

PHY Comparison between Constant and Variable Link Rate

Constant Link Rates [iDP]



Variable Link Rate from Pixel Clock



	Constant Link Rate (iDP)	Variable Link Rate
Architectural Concept	From the optimized High Speed Signaling	From Legacy Video Interface
Link Rates	Pixel Clock Decoupled	Pixel Clock Coupled tightly
Link Stability	Steady and Uninterruptible	Unstable and interruptible by Pixel Clock Variation/Change

PHY Comparison between Constant and Variable Link Rate

- **Constant Link Rate (iDP): Link Symbol Clock generated from a stable, jitter-free reference clock (e.g., crystal oscillator)**
- **Variable Link Rate : Link Symbol Clock generated using pixel clock as a reference clock**

Signal Integrity : Constant (iDP) >= Variable Link Rate

- At High Speed Signaling, the lowest jitter clock is a key technology to make a bigger eye-opening at the same conditions.

Every proven high speed signaling is using constant link rate.



Allow to use the less jittery reference clock.

PHY Comparison between Constant and Variable Link Rate

- **Constant Link Rate (iDP): Link Symbol Clock** generated from a stable, jitter-free reference clock (e.g., crystal oscillator)
- **Variable Link Rate** : Link Symbol Clock generated using pixel clock as a reference clock

Maximum Link Rate : Constant (iDP) \geq Variable Link Rate

The jitter of reference clock defines the maximum link rate at high speed signaling , an Constant link rate can use less jittery reference clock at any scenario.

Constant Link Rate (iDP) can support higher link rates at any scenario compared to a variable link rate(from a pixel clock).

DP1.2 =5.4Gbps

USB 3.0 =5Gbps

SATA = 6Gbps

Only iDP based on a proven technology.

PHY Comparison between Constant and Variable Link Rate

- **Constant Link Rate (iDP):** Link Symbol Clock generated from a stable, jitter-free reference clock (e.g., crystal oscillator)
- **Variable Link Rate :** Link Symbol Clock generated using pixel clock as a reference clock

Link Stability during video format change: Constant (iDP) >> Variable Link Rate
Pixel CLK is bound to change at any time in ATSC/DVB Application. Especially problematic for MEMC based 120-/240-Hz frame rate conversion algorithm implementation. With a variable link rate, the display should be turned off during channel / mode / input changes and it requires new Clock Recovery/Symbol Lock Sequence , if any pixel clock changes.



Only iDP (Constant Link Rate) can allow a seamless transition during channel/mode/input changes including pixel frequency variations.

THANK YOU

